LogiCORE IP LTE DL Channel Encoder v3.0

XMP023 April 2, 2014 **Product Brief**

Introduction

The Xilinx® LogiCORE™ IP LTE DL Channel Encoder core provides designers with an LTE Downlink Channel Encoding block for the *3GPP TS 36.212 v9.0.0 Multiplexing and Channel Coding* specification.

Additional Documentation

A full product guide is available for this core. Access to this material can be requested by clicking on this registration link: www.xilinx.com/member/lte_dl_channel_enc_eval/index.htm.

Features

- Channel coding for 3GPP TS 36.212 supports:
  DL-SCH, PCH, MCH, BCH, CFI, HI, and DCI
- Bit-accurate C model available
- Fully optimized for speed and area
- Fully synchronous design using a single clock

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale™ Architecture, Zynq®-7000, 7 Series
Supported User Interfaces	Can be interfaced to AXI4-Stream(2)
Provided with Core	
Design Files	Netlist
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	VHDL or Verilog Structural C Model
Supported S/W Driver	N/A
Tested Design Tools	
Design Entry Tools	Vivado® Design Suite IP Integrator
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis Tools	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

1. For a complete list of supported devices, see the Vivado IP catalog.
2. Interface similar to AXI and can be connected to an AXI4-Stream interface.
3. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The LTE DL Channel Encoder core provides a channel encoding solution for the 3GPP 36.212 specification. Figure 1 and Figure 2 respectively illustrate the main blocks in the LTE encoding chain for the two main channel types that are supported by the core. The architecture has been designed to provide efficient use of the FPGA while also offering a low bandwidth processor interface to reduce system-level overhead. Timing-critical operations are performed by the FPGA.

The interface to the core can be attached to any bus-based system. The memory-mapped interface allows for simple integration and validation within the system.

Data is processed sequentially on a transport block basis for each of the two main channel types, where the term "transport block" is used to describe a block of data originating from the MAC layer. Specific processing is applied depending on the type of input block, which is indicated as part of the control signaling provided by the MAC layer.

The following functions are supported by the core:

- CRC
  - 24-bit CRC applied to DL-SCH, PCH, and MCH transport blocks
  - 16-bit CRC applied to BCH and DCI code blocks (with additional scrambling on parity bits)
- Segmentation
  - Code block segmentation applied to DL-SCH, PCH, and MCH transport blocks (that is, data that are turbo encoded), with an additional 24-bit CRC computed on each code block (in cases where segmentation produces more than one code block)
- Encoding
  - Turbo code applied to DL-SCH, PCH, and MCH data
  - Convolutional code applied to BCH and DCI data (single code block)
- Rate Matching
  - Applied on a code block basis to DL-SCH, PCH, MCH, BCH, and DCI data. This function performs appropriate puncturing according to the AMC parameters and redundancy version.
  - Data output on a code block basis for the DL-SCH, PCH, and MCH channels.
- Control Format Indicator Generation
  - The HI or CFI coded outputs are generated according to the type indicated from the control signaling from the MAC layer.

Control and Broadcast Channel Processing

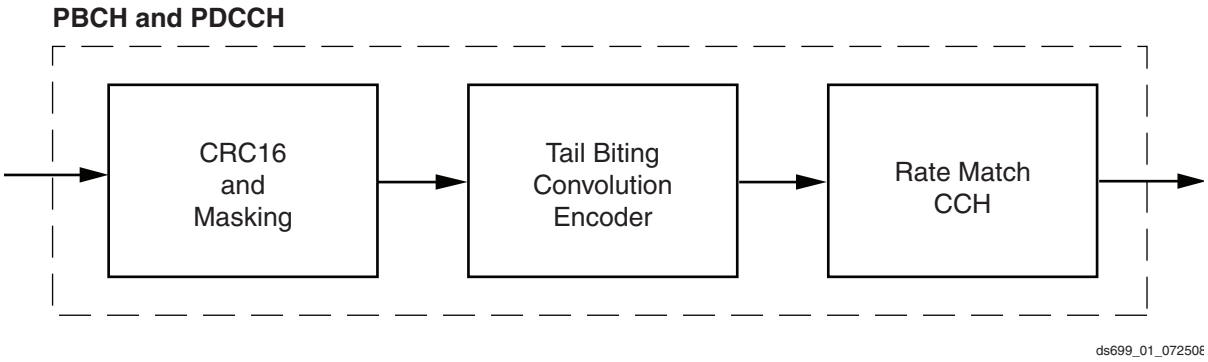

Figure 1: **Downlink Channel Processing for BCH and DCI -CCH Channel Stream**

Shared, Paging, and Multicast Channel Processing

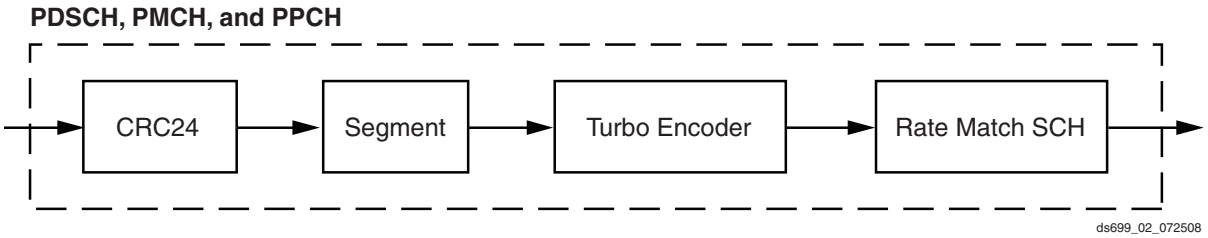

Figure 2: **Downlink Channel Processing for DL-SCH, PCH and MCH -SCH Channel Stream**

Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Turbo Code LogiCORE IP License Terms. The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the LTE DL Channel Encoder product web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

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Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/02/2014	4.0	Characterization data link added to PG069.
12/18/2013	4.0	Added UltraScale architecture support.
03/20/2013	4.0	Updated for core for Vivado only.
08/02/2012	3.5	Document update.
07/25/2012	3.4	Updated for Vivado 2012.2.
01/18/2012	3.3	Updated for ISE Release 13.4.
08/152/2011	3.2	Updated to include web registration information.
06/22/2011	3.1	Added support for 7 Series devices and ISE Design Suite 13.2.
04/19/2010	3.0	Added support for latest Spartan-6 and Virtex-6 device variants.
04/24/2009	2.0	Virtex-6 and Spartan-6 support added. Addition of Transport block start and end signals. Modification to CRC output to support v8.5 of RNTI scrambling.
09/19/2008	1.0	Xilinx initial release.

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