LogiCORE IP LTE PUCCH Receiver v2.0

XMP156 March 20, 2013 **Product Brief**

Introduction

The Xilinx LogiCORE™ IP LTE Physical Uplink Control Channel (PUCCH) Receiver implements an AXI4-Stream compliant, high-performance, optimized block for the 3GPP TS 36.211 v9.0.0 Physical uplink control channel. The data and control for the core are input on independent AXI4-Stream channels as slave interfaces and the resulting status is output on an AXI4-Stream master interface.

Additional Documentation

A product guide is available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/pucch_eval/index.htm.

Features

- AXI4-Stream compliant interfaces
- Physical Uplink Control Channel Receiver for 3GPP TS 36.211 v9.0.0
- TDD/FDD compliant
- Supports 1, 2 or 4 antenna operation
- Supports all format types including Mixed Format
- Supports both normal and shortened slots
- Supports normal and extended Cyclic Prefix
- Fully optimized for speed and area
- Fully synchronous design using a single clock
- Bit-accurate C model
- Compliant with all required conformance tests (3GPP TS36.141 Base Station conformance testing)
- Customer demonstration test bench
- Delivered by Xilinx Vivado™ Design Suite

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq™-7000, Virtex®-7, Kintex™-7, Artix™-7
Supported User Interfaces	AXI4-Stream
Provided with Core	
Design Files	Encrypted RTL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided
Simulation Model	VHDL Behavioral VHDL or Verilog Structural C Model
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado™ Design Suite System Generator for DSP
Simulation	Mentor Graphics Questa® SIM Vivado Simulator
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete listing of supported devices, see the Vivado IP Catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Applications

The LTE PUCCH Receiver core provides a receiver solution for the 3GPP 36.211 Physical Uplink Control Channel (PUCCH). The architecture has been designed to provide efficient use of the FPGA resources while also offering a low bandwidth processor interface to reduce system-level overhead. Timing critical operations are performed by the FPGA.

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the LTE PUCCH product web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

References

1. 3GPP TS 36.211, v9.0.0 (2009-12), “Physical Channels and Modulation (Release 9)”
2. 3GPP TS 36.212, v9.0.0 (2009-12), “Multiplexing and channel coding (Release 9)”

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/01/2011	1.0	First release of the core.
08/15/2011	1.1	Updated to include web registration information.
03/20/2013	2.0	Updated core version for Vivado.

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