LogiCORE IP LTE UL Channel Decoder v3.0

PB005 August 15, 2011 **Product Brief**

Introduction

The Xilinx LogiCORE™ IP LTE Uplink Channel Decoder implements an AXI4 compliant, high-performance, optimized decoder block for the 3GPP TS 36.212 v9.3.0 Uplink Shared Channel (UL-SCH).

Features

- AXI4 compliant interfaces
- Uplink Shared Channel decoder for 3GPP TS 36.212 v9.3.0
- Transport Block Decoder and Channel Quality Information Decoder sub-components can be generated as stand-alone cores
- TDD/FDD compliant
- Support for on or off chip codeword buffering
- Integrated descrambling
- Integrated LLR calculation
- Fully decoupled decoding chains
- Fully optimized for speed and area
- Fully synchronous design using a single clock
- Bit Accurate C model
- Customer demonstration test bench
- User guide available for detailed information on core usage
- For use with Xilinx CORE Generator™ tool 13.2

LogiCORE IP Facts	
Core Specifics	
Supported Device Family(1)	Virtex®-7, Kintex™-7, Artix™-7, Zynq™-7000, Virtex-6, Virtex-5
Supported User Interfaces	AXI4, AXI4-Stream
Provided with Core	
Documentation	Product Specification User Guide
Design Files	Netlist and C model
Example Design	N/A
Test Bench	VHDL
Constraints File	N/A
Simulation Model	Verilog and VHDL UNISIM model, C model and MATLAB model
Tested Design Tools	
Design Entry Tools	CORE Generator tool 13.2
Simulation(2)	Mentor Graphics ModelSim Cadence Incisive Enterprise Simulator (IES) Synopsys VCS and VCS MX ISim
Synthesis Tools	XST 13.2
Support	
Provided by Xilinx, Inc.	

1. For the complete list of supported devices, see the release notes for this core.
2. For the supported version of the tools, see the ISE Design Suite 13: Release Notes Guide

Functional Description

The LTE UL Channel Decoder core provides a decoder solution for the 3GPP 36.212 uplink shared channel. The architecture has been designed to provide efficient use of the FPGA resources while also offering a streaming interface to reduce system-level overhead.

Additional Documentation and Supporting Materials

A full data sheet and additional supporting materials (C models and accompanying user guide documentation) are available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/lte_ul_channel_dec_eval/index.htm.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

See the IP Release Notes Guide (XTP025) for further information on this core.

For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Ordering Information

The LTE UL Channel Decoder core is provided under the SignOnce IP Site License and can be generated using the Xilinx CORE Generator software v13.2. The CORE Generator software is shipped with Xilinx ISE Design Suite software.

To access the full functionality of the core, including simulation and FPGA bitstream generation, a full license must be obtained from Xilinx. For more information, visit the LTE UL Channel Decoder product page.

This product requires the separately licensed 3GPP LTE Turbo Decoder LogiCORE. For more information, see the 3GPP LTE Turbo Decoder product page

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/22/11	1.0	Initial Xilinx release.
08/15/11	1.1	Updated to include web registration information.

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