

Introduction

The Xilinx® LogiCORE™ IP LTE Uplink Channel Decoder implements an AXI4 compliant, high-performance, optimized decoder block for the 3GPP TS 36.212 v9.3.0 Uplink Shared Channel (UL-SCH).

Additional Documentation

A full product guide is available for this core. Access to this material can be requested by clicking on this registration link: www.xilinx.com/member/lte_ul_channel_dec_eval/index.htm.

Features

- AXI4 compliant interfaces
- Uplink Shared Channel decoder for 3GPP TS 36.212 v9.3.0
- Transport Block Decoder and Channel Quality Information Decoder sub-components can be generated as stand-alone cores
- TDD/FDD compliant
- Support for on or off chip codeword buffering
- Integrated descrambling
- Integrated LLR calculation
- Fully decoupled decoding chains
- Fully optimized for speed and area
- Fully synchronous design using a single clock
- Bit accurate C model
- Customer demonstration test bench

LogiCORE IP Facts	
Core Specifics	
Supported Device Family ⁽¹⁾	UltraScale+™ UltraScale™ Zynq®-7000 All Programmable SoC 7 Series
Supported User Interfaces	AXI4, AXI4-Stream
Provided with Core	
Design Files	Encrypted VHDL
Example Design	Not provided
Test Bench	VHDL
Constraints File	Not provided
Simulation Model	Encrypted VHDL C model and MATLAB model
Tested Design Tools⁽²⁾	
Design Entry Tools	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide .
Synthesis Tools	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For the complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).

Functional Description

The LTE UL Channel Decoder core provides a decoder solution for the 3GPP 36.212 uplink shared channel. The architecture has been designed to provide efficient use of the FPGA resources while also offering a streaming interface to reduce system-level overhead.

Technical Support

Xilinx provides technical support at the [Xilinx Support web page](#) for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the [Xilinx Support web page](#).

Licensing and Ordering Information

This Xilinx LogiCORE™ IP module is provided under the terms of the [Xilinx Turbo Code LogiCORE IP License Terms](#). The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your [local Xilinx sales representative](#) for information about pricing and availability.

For more information, visit the LTE UL Channel Decoder [product web page](#).

Information about other Xilinx LogiCORE IP modules is available at the [Xilinx Intellectual Property](#) page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your [local Xilinx sales representative](#).

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Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
10/05/2016	4.0	PG163 test bench chapter updated.
11/18/2015	4.0	Added support for UltraScale+ families.
04/02/2014	4.0	Characterization data link added to PG163.
12/18/2013	4.0	<ul style="list-style-type: none"> Revision number advanced to 4.0 to align with core version number. Added UltraScale architecture support.
03/20/2013	1.2	Updated for core version. Removed ISE® information.
08/15/2011	1.1	Updated to include web registration information.
06/22/2011	1.0	Initial Xilinx release.

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