Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions (v2.3)

DS176 June 24, 2015 **Advance Product Specification**

Introduction

The Xilinx® Zynq®-7000 All Programmable SoC and 7 series FPGAs memory interface solutions cores provide high-performance connections to DDR3 and DDR2 SDRAMs, QDR II+ SRAM, RLDRAM II/RLDRAM 3, and LPDDR2 SDRAM.

DDR3 and DDR2 SDRAMs

This section discusses the features, applications, and functional description of Xilinx 7 series FPGAs memory interface solutions in DDR3 and DDR2 SDRAMs. These solutions are available with an optional AXI4 slave interface.

DDR3 SDRAM Features

- Component support for interface widths up to 72 bits
- Single and dual rank UDIMM, RDIMM, and SODIMM support
- DDR3 (1.5V) and DDR3L (1.35V)
- 1, 2, 4, and 8 Gb density device support
- 8-bank support
- x8 and x16 device support
- 8:1 DQ:DQS ratio support
- Configurable data bus widths (multiples of 8, up to 72 bits)
- 8-word burst support
- Support for 5 to 14 cycles of column-address strobe (CAS) latency (CL)
- On-die termination (ODT) support
- Support for 5 to 10 cycles of CAS write latency
- ZQ calibration – initial and periodic (configurable)
- Write leveling support for DDR3 (fly-by routing topology required for DDR3 component designs)
- JEDEC®-compliant DDR3 initialization support
- Source code delivery in Verilog and VHDL (top-level files only)
- 4:1 and 2:1 memory to FPGA logic interface clock ratio
- ECC support
- I/O Power Reduction option reduces average I/O power by automatically disabling DQ/DQS IBUFs and internal terminations during writes and periods of inactivity
- Internal V_{REF} support
- Multicontroller support for up to eight controllers
- Two controller request processing modes:
  - Normal: reorder requests to optimize system throughput and latency
  - Strict: memory requests are processed in the order received

LogiCORE™ IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq®-7000All Programmable SoC, Virtex®-7(2), Kintex®-7(2), Artix®-7
Supported Memory	DDR3 Component and DIMM, DDR2 Component and DIMM, QDR II+, RLDRAM II, RLDRAM 3, and LPDDR2 SDRAM Components
Resources	See Table 1.
Provided with Core	
Documentation	Product Specification User Guide
Design Files	Verilog, VHDL (top-level files only)
Example Design	Verilog, VHDL (top-level files only)
Test Bench	Not Provided
Constraints File	XDC
Supported S/W Driver	N/A
Tested Design Flows(3)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis(4)	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page.	

Notes:

1. For a complete listing of supported devices, see the release notes for MIG.
2. See the *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics* or the *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics* for performance information.
3. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.
4. The standard synthesis flow for Synplify is not supported for the core.

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DDR2 SDRAM Features

- Component support for interface widths up to 64 bits
- Single rank UDIMM, RDIMM, and SODIMM
- 1 and 2 Gb density device support (additional densities supported in the MIG tool using the Create Custom Part feature)
- 4- and 8-bank support
- x8 and x16 device support
- 8:1 DQ:DQS ratio support
- Configurable data bus widths (multiples of 8, up to 72 bits)
- 8-word burst support
- Support for 3 to 6 cycles of column address strobe (CAS) latency
- On-die termination (ODT) support
- JEDEC-compliant DDR2 initialization support
- Source code delivery in Verilog and VHDL (top-level files only)
- 4:1 and 2:1 memory to FPGA logic interface clock ratio
- ECC support
- I/O Power Reduction option reduces average I/O power by automatically disabling DQ/DQS IBUFs and internal terminations during writes and periods of inactivity
- Internal V_{REF} support
- Two controller request processing modes:
  - Normal: Reorder requests to optimize system throughput and latency
  - Strict: Memory requests are processed in the order received
- Multiple controllers per FPGA supported running the MIG tool multiple times

Applications

Typical applications for the Xilinx 7 series FPGAs memory interface solutions include DDR3 SDRAM and DDR2 SDRAM interfaces.

Figure 1 shows a high-level block diagram of the 7 series FPGAs memory interface solution connecting a user design to a DDR2 or DDR3 SDRAM device. The physical layer (PHY) side of the design is connected to the DDR2 or DDR3 SDRAM device through FPGA I/O blocks (IOBs), and the user interface side is connected to the user design through FPGA logic. For more details regarding the design, see the *Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586) [Ref 2].

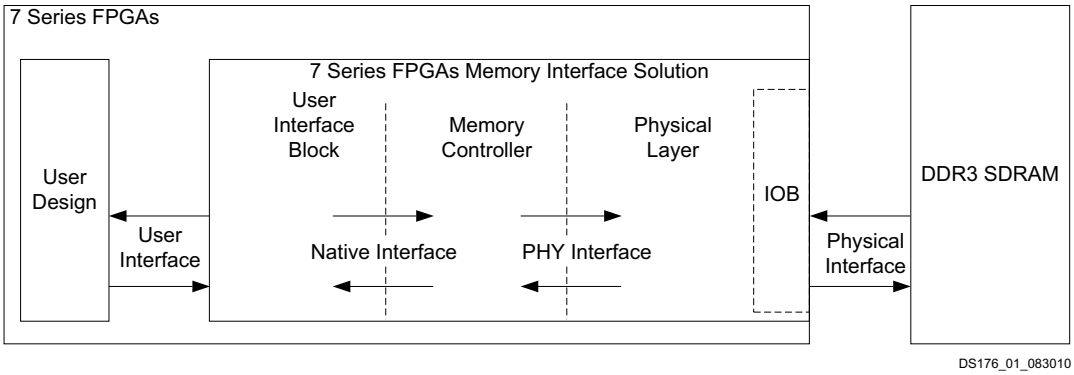

Figure 1: **DDR2/DDR3 SDRAM Memory Interface Solution**

Functional Description

As shown in Figure 1, the top-level functional blocks of the Xilinx 7 series FPGAs memory interface solution include:

- The User Interface block:
  - Presents the user interface to a user design
  - Provides a simple and user-friendly alternative to the native interface
  - Buffers read and write data
  - Reorders read return data to match the request order
  - Presents a flat address space and translates it to the addressing required by the SDRAM
- The Memory Controller block:
  - Receives requests from the user design
  - Reorders requests to minimize dead states for maximum SDRAM performance
  - Manages SDRAM row/bank configuration
  - Performs high-level SDRAM management such as refresh and activate/precharge
- The PHY block:
  - Interfaces with the Memory Controller block over a simple interface and translates the signals into the actual signals sent to the SDRAM, and vice versa
  - Translates and synchronizes control and data over various clock domains
  - Initializes the SDRAM
  - Performs write leveling for DDR3 (fly-by routing topology required for component designs)
  - Performs calibration to center align capture clocks with read data

Figure 1 also shows a user design connecting to the memory interface. An example user design is provided with the core. For more details regarding the design, see the *Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586) [Ref 2].

AXI4 Slave Interface Features

These features are optional and selectable using the MIG GUI:

- AMBA® AXI4 slave-compliant memory-mapped interface
- AXI4-Lite interface support for ECC control and status registers
- 1:1 clock rate to the controller

- AXI4 interface data widths can be 64, 128, 256, or 512 bits to correspond with memory data widths of 8, 16, 32, 64, or 72 bits
- Parameterized address width support
- Support for incremental (INCR) burst up to 256 data beats
- WRAP burst support
- Multicontroller support for up to eight DDR3 SDRAM controllers

QDR II+ SRAM

This section discusses the features, applications, and functional description of Xilinx 7 series FPGAs memory interface solutions in QDR II+ SRAMs.

Features

- QDR II+ SRAM device support
- x18 and x36 memory width support
- Configurable data bus widths (x18, x36)
- 2-word and 4-word burst support
- Source code delivery in Verilog and VHDL (top-level files only)
- 2:1 memory to FPGA logic interface clock ratio
- 2.0-cycle and 2.5-cycle read latency support
- Fixed latency mode support
- Internal V_{REF} support
- Multicontroller support for up to eight controllers

Applications

QDR II+ SRAMs offer high-speed data transfers on separate read and write buses on the rising and falling edges of the clock. These memory devices are used in high-performance systems as temporary data storage, such as:

- Look-up tables in networking systems
- Packet buffers in network switches
- Cache memory in high-speed computing
- Data buffers in high-performance testers

Figure 2 shows a high-level block diagram of the 7 series FPGAs memory interface solution connecting a user design to a QDR II+ SRAM device.

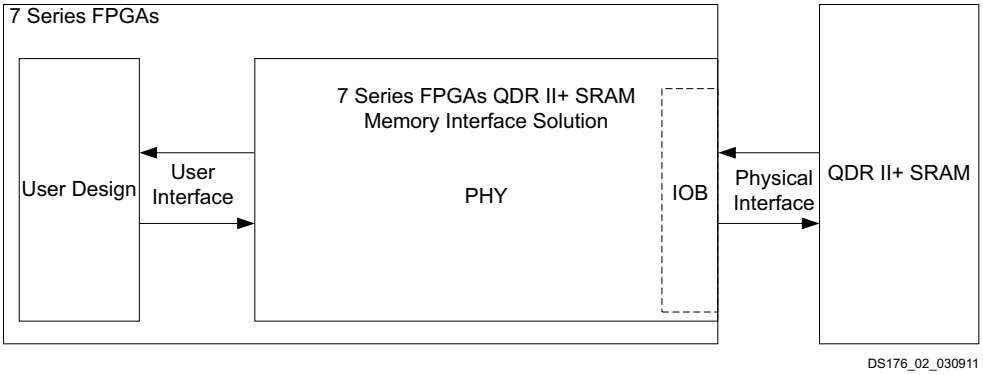

Figure 2: **QDR II+ SRAM Memory Interface Core**

Functional Description

As shown in Figure 2, the top-level functional block is composed of a PHY that interfaces to the user and to the QDR II+ SRAM device. The PHY block:

- Translates simple user read and write commands to conform to QDR II+ SRAM protocol
- Enables the user to provide up to one read and one write transaction per clock cycle for maximum throughput
- Performs calibration to center align clocks with data
- Returns data to the user with a corresponding valid signal
- Translates and synchronizes over various clock domains
- Implements an optimized half-frequency design that eliminates the need for a memory controller

For more details regarding the design, see the *Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586) [Ref 2] provided with the core.

RLDRAM II/RLDRAM 3

This section discusses the features, applications, and functional description of Xilinx 7 series FPGAs memory interface solutions in RLDRAM II and RLDRAM 3 devices.

RLDRAM II Features

- RLDRAM II common I/O (CIO) memory device support
- x18 and x36 memory width support
- Configurable data bus widths (x18, x36, x72)
- 4-word and 8-word burst support
- Configuration 1, 2, 3 support
- Address Multiplexing Mode support
- ODT support
- Source code delivery in Verilog and VHDL (top-level files only)
- 2:1 memory to FPGA logic interface clock ratio
- Internal V_{REF} support

- Multicontroller support for up to eight controllers

RLDRAM 3 Features

- x18 and x36 memory width support
- Configurable data bus widths (x18, x36, x72)
- 2-word, 4-word, and 8-word burst support
- Address Multiplexing Mode support
- ODT support
- Source code delivery in Verilog only
- 4:1 memory to FPGA logic interface clock ratio
- Internal V_{REF} support

Applications

RLDRAM II and RLDRAM 3 devices are used in high-performance systems as temporary data storage, such as:

- Look-up tables in networking systems
- Packet buffers in network switches
- Cache memory in high-speed computing
- Data buffers in high-performance testers

Figure 3 shows a high-level block diagram of the 7 series FPGAs memory interface solution connecting a user design to an RLDRAM device. The physical layer is connected to the RLDRAM device through FPGA IOBs, and the user interface is connected to the user design through FPGA logic.

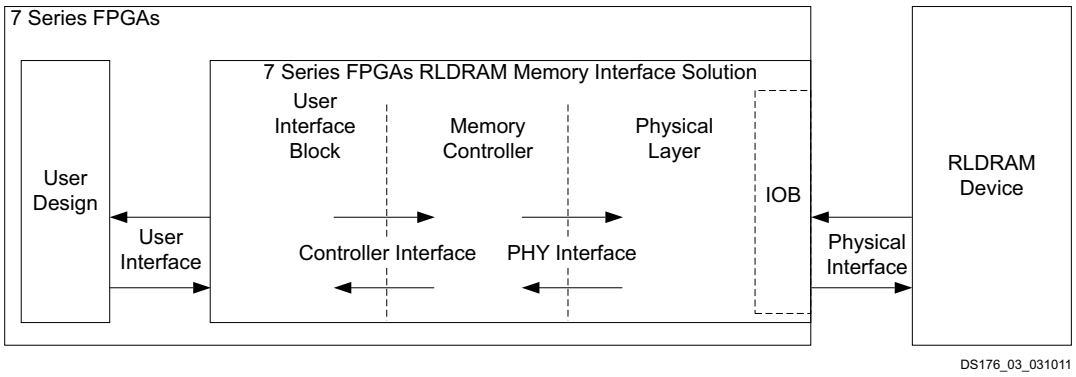

Figure 3: **RLDRAM Memory Interface Core**

Functional Description

As shown in Figure 3, the top-level functional blocks of the RLDRAM memory interface solution include:

- The User Interface block:
  - Presents the user interface to a user design
  - Buffers commands and write data
- The Memory Controller block:
  - Receives requests from the user design
  - Processes commands in order and adheres to memory specifications
  - Performs high-level SDRAM management, such as refresh, and controls bank access

- The Physical Layer (PHY) block:
  - Interfaces with the Memory Controller block over a simple interface and translates the signals into the actual signals sent to the RLDRAM, and vice versa.
  - Performs memory initialization sequence.
  - Performs calibration to center align clocks with data
  - Returns data to the user with a corresponding valid signal

For more details regarding the design, see the *Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586) [Ref 2] provided with the core.

LPDDR2 SDRAM

This section discusses the features, applications, and functional description of Xilinx 7 series FPGAs memory interface solutions in LPDDR2 SDRAMs.

LPDDR2 SDRAM Features

- Component support for interface widths up to 32 bits
- 2 and 4 Gb density device support
- 8-bank support
- x16 and x32 device support
- 8:1 DQ:DQS ratio support
- 8-word burst support
- JEDEC-compliant LPDDR2 SDRAM initialization support
- Source code delivery in Verilog
- 2:1 memory to FPGA logic interface clock ratio
- Internal V_{REF} support
- Two controller request processing modes:
  - Normal: reorder requests to optimize system throughput and latency
  - Strict: memory requests are processed in the order received

Applications

Typical applications for the Xilinx 7 series FPGAs memory interface solutions include LPDDR2 SDRAM interfaces.

Figure 4 shows a high-level block diagram of the 7 series FPGAs memory interface solution connecting a user design to a LPDDR2 SDRAM device. The physical layer (PHY) side of the design is connected to the LPDDR2 SDRAM device through FPGA I/O blocks (IOBs), and the user interface side is connected to the user design through FPGA logic. For more details regarding the design, see the *Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586) [Ref 2] provided with the core.

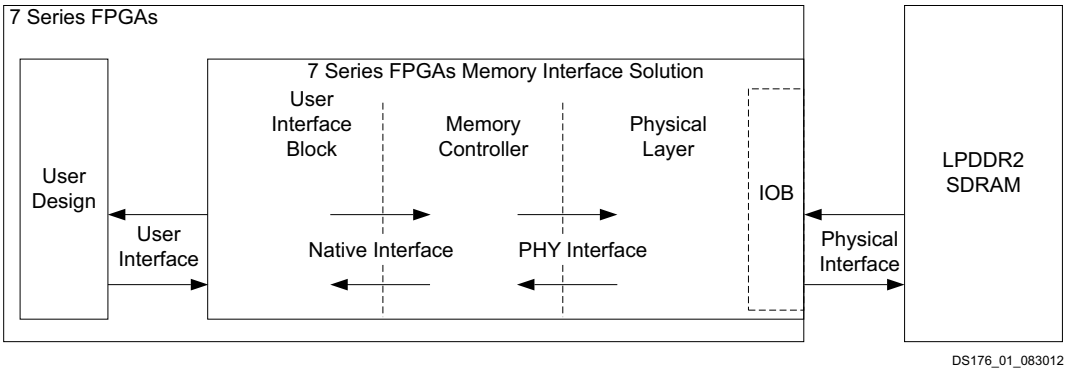

Figure 4: **LPDDR2 SDRAM Memory Interface Solution**

Functional Description

As shown in Figure 4, the top-level functional blocks of the Xilinx 7 series FPGAs memory interface solution include:

- The User Interface block:
  - Presents the user interface to a user design
  - Provides a simple and user-friendly alternative to the native interface
  - Buffers read and write data
  - Reorders read return data to match the request order
  - Presents a flat address space and translates it to the addressing required by the SDRAM
- The Memory Controller block:
  - Receives requests from the user design
  - Reorders requests to minimize dead states for maximum SDRAM performance
  - Manages SDRAM row/bank configuration
  - Performs high-level SDRAM management such as refresh and activate/precharge
- The Physical Layer (PHY) block:
  - Interfaces with the Memory Controller block over a simple interface and translates the signals into the actual signals sent to the SDRAM, and vice versa.
  - Translates and synchronizes control and data over various clock domains
  - Initializes the SDRAM
  - Performs calibration to center align capture clocks with read data

Figure 4 also shows a user design connecting to the memory interface. For more details regarding the design, see the *Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586) [Ref 2] provided with the core.

General Specifications

For more details regarding specific banking, pin location, and internal clock resource requirements for all cores, see the *Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586) [Ref 2].

Resource Utilization

Table 1: **Resource Utilization for 7 Series FPGAs**

Product[1]	LUTs	Flip-Flops	BUFG	PLLE2	MMCM	Block RAM
7 Series FPGAs DDR3 SDRAM[2]	14,016	9,019	4[3][4]	1	2[3]	2
7 Series FPGAs DDR2 SDRAM[2]	9,267	6,038	2	1	1	0
7 Series FPGAs QDR II+SRAM	3,209	2,568	2	1	1	0
7 Series FPGAs RLDRAM II	6,261	4,519	2	1	1	7
7 Series FPGAs RLDRAM 3	9,039	7,950	2	1	1	12
7 Series FPGAs LPDDR2 SDRAM	3,952	3,285	2	1	1	0

Notes:

1. Resource utilization can change depending on the options chosen, memory device used, or both. Resource information is provided for 72-bit DDR3 SDRAM, 72-bit DDR2 SDRAM, 36-bit QDR II+ SRAM, 72-bit RLDRAM II, 72-bit RLDRAM 3, and 32-bit LPDDR2 SDRAM interfaces.
2. UDIMM 72-bit designs (ECC disabled).
3. For design frequencies > 667 MHz, three BUFGs and two MMCM are utilized in the design. For design frequencies < 667 MHz, only two BUFGs and one MMCM are utilized in the design.
4. One BUFG used for the clock during write calibration.

Verification

Xilinx 7 series FPGAs memory interface solutions cores have been verified in simulation. Verification tests include:

- Initialization sequence
- Read calibration
- Memory read operation
- Memory write operation
- Row/bank management
- Write leveling

Additional Resources

This section provides additional information related to this data sheet:

1. JEDEC Standard JESD79-3E: DDR3 SDRAM, JEDEC Solid State Technology Association
   JEDEC Standard JESD79-2F: DDR2 SDRAM Specification, JEDEC Solid State Technology Association
   JEDEC web page

This Xilinx document can be located on the MIG Solution Center Documentation page:

2. *Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586)
3. 7 Series FPGAs Data Sheets
4. *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics* (DS183)
5. *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics* (DS182)
6. *ISE to Vivado Design Suite Migration Guide* (UG911)
7. *Vivado Design Suite User Guide: Designing with IP* (UG896)

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Revision History

The following table shows the revision history for this document:

Date	Version	Revision
06/24/2015	2.3	• Vivado Design Suite release for MIG v2.3.
04/01/2015	2.3	• Vivado Design Suite release for MIG v2.3. • Updated Table 1: Resource Utilization for 7 Series FPGAs.
11/19/2014	2.3	• Vivado Design Suite release for MIG v2.3.
10/01/2014	2.2	• Vivado Design Suite release for MIG v2.2.
06/04/2014	2.1	• Vivado Design Suite release for MIG v2.1. • Updated Table 1: Resource Utilization for 7 Series FPGAs.
12/18/2013	2.0	• Vivado Design Suite release for MIG v2.0. • Updated doc title.
10/02/2013	2.0	• Vivado Design Suite release for MIG v2.0. • Updated simulation row in IP Facts table.
06/19/2013	2.0	Vivado Design Suite release for MIG v2.0. Revision number advanced to 2.0 to align with core version number.
03/20/2013	1.8	• ISE 14.5 and Vivado Design Suite releases for MIG v1.9. • Moved Resource table into a separate Resource section. • Updated 7 Series FPGAs DDR3 SDRAM in Table 1 Resource Utilization. • Added LPDDR2 SDRAM content.
12/18/2012	1.7	• ISE 14.4 and Vivado 2012.4 Design Suite releases for MIG v1.8. • Added 8 Gb to DDR3 SDRAM feature. • Added VHDL support.
10/16/2012	1.6	ISE 14.3 and Vivado 2012.3 Design Suite releases for MIG v1.7. Added RLDRAM 3 content.
07/25/2012	1.5	ISE 14.2 and Vivado 2012.2 Design Suite releases for MIG v1.6.
04/24/2012	1.4	ISE 14.1 tool release for MIG v1.5. • Added VHDL source code for top-level files for all memory devices • For DDR3 and DDR2 SDRAM, added: I/O Power Reduction option, AXI4-Lite interface support for ECC control and status registers, and 72-bit data width.
01/18/2012	1.3	ISE 13.4 tool release for MIG v1.4. • For DDR3 SDRAM: Added support for 4 Gb density, DDR3L (1.35 V), and dual rank UDIMM, RDIMM, and SODIMM. Removed support for AXI4-Lite interface and 72-bit data width. • Added DDR2 SDRAM support.

Date	Version	Revision
10/19/2011	1.2	ISE 13.3 software release for MIG v1.3. • Added Resources to the IP Facts table. • For DDR3 SDRAM, added support for up to eight controllers, added 2:1 as an interface clock ratio, added AXI4-Lite interface support, and added 72 as a memory data width option. • For QDR II+ SRAM, added support for 2-word bursts and support for up to eight controllers. • For RLDRAM II, added support for Address Multiplexing Mode and support for up to eight controllers.
06/22/2011	1.1	ISE 13.2 software release. Added RLDRAM II support throughout document. Added single rank UDIMM support bullet to DDR3 SDRAM Features, page 1. Added internal V_{REF} support.
03/01/2011	1.0	Initial Xilinx release.

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