MPEG-4 Simple Profile Encoder v1.2

DS511 v1.8 April 14, 2008 **Product Specification**

Introduction

The Xilinx® MPEG-4 Part 2 Simple Profile Encoder (MPEG-4 Encoder) core is a fully functional VHDL design implemented on a Xilinx FPGA. The MPEG-4 Encoder core accepts uncompressed video and generates compressed bit streams based on the *"Information Technology–Generic Coding of Audio Visual Objects-Part 2 Visual"* section of the ISO/IEC 14496-2 standard.

This document describes the core functionality, its input/output structure, and how the core is used.

Features

- Supported FPGA families: Virtex®-5, Virtex-4, Virtex-II Pro, Virtex-II, Spartan®-3, and Spartan-3A
- MPEG-4 Part 2 Simple Profile Level 5 (Standard Definition)
- User-defined maximum frame size
- Directional squared motion estimation with early stop
- ½ pixel motion estimation
- 4:2:0: YUV processing
- Single external frame buffer; predicted frame processing
- Variable length coding in hardware
- Host interface for rate control algorithm
- Support for full MPEG-4 header

Applications

Some of the key applications for the MPEG-4 Encoder core are defined below.

Automotive

Today's automobile makers are incorporating the latest technologies, including Global Positioning Systems (GPS) and collision avoidance systems, which require drivers to be able to see video sequences in real-time to make split-second decisions. Video compression technology has become an important part of the auto industry's infrastructure, and the MPEG-4 technology enhances the overall product and data transmission requirements.

Medical Imaging

Medical imaging, processing, and archival benefit greatly from the use of MPEG-4 compression techniques for both still and video images in non-clinical application setting.

Industrial and Security

MPEG-4 compression algorithms are an excellent resource for applications that require video sequences from multiple locations to be sent to a central location for processing, for example, video sequences captured from a variety of locations within an office building or manufacturing plant to a security control room.

Broadcasting

MPEG-4 technology provides the broadcast community with an effective way to transmit information in a highly compressed format that can deliver various levels of high-quality video information both inside and outside the studio. In addition, the invention of HDTV required a way to compress video signals to be able to occupy the same analog channel that existed for SDTV.

Military

Video surveillance from military aircraft necessitates sending valuable video imagery over wireless communication channels. These types of applications rely strongly on effective video compression techniques that can operate at different resolutions based on the accuracy and image quality required.

Video Conferencing

MPEG-4 encoding and video compression allow for the transmission of high-quality video to multiple sites in real time, reducing travel time and overall costs.

Streaming Video

Delivering video information through streaming video is an important aspect of internet communication, and combining MPEG-4 technology with the host of other internet technologies enhances the overall internet experience.

Video Messaging

Cellular telephone technology has gained a significant share of the consumer market over the last decade and continues to expand into other areas, including video. Because the MPEG4 Encoder has the capability to compress low-resolution images very effectively, the MPEG-4 algorithm is a natural fit for small-screen applications.

Feature Summary

- **MPEG-4 Simple Profile Encoder standard**. The MPEG-4 Encoder core follows the International Standards Organization document number ISO/IEC 14496-2:199/Amd.1:2000(E) from the ISO/IEC JTC 1/SC 29/WG 11 Coding of Moving Pictures and Audio group. This document may be purchased from the MPEG web site at http://www.iso.ch/iso/en/prods-services/ISOstore/store.html.
- **User-defined maximum frame size**. The MPEG-4 Encoder core can operate at different resolutions, from Standard Definition (720 by 576) to QCIF (176 by 144). The frame size directly affects the total amount of on-chip memory, or block RAMs, required.
- **Directional squared motion estimation and compensation**. The MPEG-4 Encoder has a motion estimation and motion compensation module in the design to produce motion vectors for the compressed bitstream. It also will use these vectors to access a locally stored memory containing macroblocks of the previously decoded frame. These macroblocks will be used as a reference to operate on the incoming residual processed data. The motion estimation used is a directed search with early stop condition.
- **1/2 pixel motion estimation**. The MPEG-4 Encoder core uses 1/2 pixel motion estimation for motion vectors using integer pixel best match and then 1/2 pixel search to refine the best motion vector match.
- **YUV processing**. The structure of the macroblock demands that the processing used in an MPEG-4 system, or MPEG system, necessitates 4:2:0 YUV processing. The color channels sample at exactly half the rate in both the horizontal and vertical directions as they relate to the Y channel. Therefore, for every U and V pixel there are four Y pixels. The spatial relationship among the three channels has been documented in many MPEG articles.
- **Single external frame buffer—predicted frame processing**. The MPEG-4 Encoder structure uses frame differences to create the residual macroblocks of information. The Encoder adds back the expanded bitstream to the appropriate motion compensated macroblock previously stored in an external frame buffer.
- **Variable length coding in hardware**. The core receives the uncompressed bitstream from a source and proceeds to encode the information and present the information in a discernible manner to the appropriate modules. The encoding process involves an production of variable length code words for motion vectors and residual data.
- **Rate control**. The MPEG-4 Encoder uses statistics generated internally to the core to update the quantization on a frame by frame basis. This allows for external rate control algorithms to be executed by a host processor and adjust the quantization based on varying bandwidth conditions. In addition, scene complexity and motion will have an effect on the bits produced and can be changed on a frame basis.

- **Support for full MPEG-4 header**. The MPEG-4 Encoder core supports full MPEG-4 header for elementary stream; short header is not supported in this release.
- **Discrete Cosine Transform**. The core implements the standard compliant Discrete Cosine Transform (DCT) and Inverse Discrete Cosine Transform (IDCT), which is used to transform an eight-by-eight block of video information from the frequency domain to the spatial domain. The data is in the frequency domain and the coefficients or residual information can be quantized and efficiently encoded for low bandwidth channels. The encoder also performs the inverse quantization and IDCT to reconstruct the same reference frame as the decoder has.
- **Macroblock processing**. The MPEG-4 Encoder core operates on a macroblock structure, a basic and important data structure of the MPEG-4 algorithm. The macroblock structure contains YUV information for a particular sub-section of the image, namely a 16-pixel by 16-pixel square. Because the chroma data representation of that block of video information is reduced in spatial frequency in both the horizontal and vertical directions, there are less informational pixels needed for the UV components (1/4 of the luma channel information for both color channels). Therefore, a macroblock is comprised of 4 luma channel eight-by-eight blocks, one U channel eight-by-eight block, and one V channel eight-by-eight block representing a 16-pixel by 16-pixel portion of the image.
- **Residual processing**. Following the motion estimation process, the information that will be encoded consists of either motion compensation vectors or residual coefficient data. The residual coefficients are sent to the Texture_Coding module where DC and AC prediction processing occurs based on picture type and macroblock location. The resulting frequency domain pixels are processed by the inverse quantization and the inverse discrete coefficient transform to convert the information back to the spatial domain, this information is used to build the next reference frame. The frequency domain pixels together with the associated motion vectors are also sent to the entropy coder which generates the final encoded bitstream.
- **8-bit input data**. For 8-bit data, the MPEG-4 Encoder requires 8-bit input data and produces 8-bit encoded bitstreams. A 32-bit pixel packed data interface is provided on the interface.
- **12-bit DTC coefficients**. For DCT transformed coefficient data, 12-bit representation is used to maintain internal bit accuracy during the execution of the two-stage separable frequency conversion operation.
- **AC/DC prediction**. The MPEG-4 standard uses different prediction modes of operation in determining the DC and AC initial values or predicted values. The core determines which mode that has to be employed, then calculates the appropriate value with the result being added to the parsed coefficient.
- **Local YUV buffer**. During the motion compensation process, macroblocks from the previous frame will be used in the construction of the current video image. In fact, the same macroblock may be used in the construction of a number of current image macroblocks. Therefore, the core has a local buffer that will contain a number of macroblocks that may be used multiple times in the motion compensation process. The local buffer concept has been employed to minimize bus bandwidth traffic.
- **Communication primitives**. The MPEG-4 Encoder core uses a variety of communication primitives, hardware-based memories, to send variable blocks of data between the different functional modules. These primitives help create a smooth processing flow between the variable number clocks needed for each module inherent in a variable length encoding scheme.
- **Bit-accurate testing**. The data generated by the MPEG-4 Encoder core has been compared to a functional C-model program to ensure bit-accurate functionality of the hardware core.

MPEG-4 Simple Profile Encoder Core Overview

The MPEG-4 Encoder provides a set of 15 precompiled configurations delivered as netlists to support specific modes of operation. The variations to the basic core involve changing the image resolution and the number of supporting bitstreams. All the configurations originate from the same VHDL file with different generic map settings. Table 1 defines the available configurations, all of which support 30 frames per second.

Table 1: **Core Configuration**

File Name (EDF)	Resolution	Description
MPEG4_SP_Encoder_V4_QCIF.edf	QCIF	Low resolution core operating at QCIF resolution for a Virtex-4 device.
MPEG4_SP_Encoder_V5_QCIF.edf	QCIF	Low Resolution Core operating at QCIF resolution for a Virtex-5 device.
MPEG4_SP_Encoder_V2P_QCIF.edf	QCIF	Low resolution core operating at QCIF resolution for a Virtex-II Pro device.
MPEG4_SP_Encoder_S3_QCIF.edf	QCIF	Low resolution core operating at QCIF resolution for a Spartan-3 device.
MPEG4_SP_Encoder_S3A_QCIF.edf	QCIF	Low Resolution Core operating at QCIF resolution for a Spartan-3A device.
MPEG4_SP_Encoder_V4_CIF.edf	CIF	Medium resolution core operating at CIF resolution for a Virtex-4 device.
MPEG4_SP_Encoder_V5_CIF.edf	CIF	Low Resolution Core operating at CIF resolution for a Virtex-5 device.
MPEG4_SP_Encoder_V2P_CIF.edf	CIF	Medium resolution core operating at CIF resolution for a Virtex-II Pro device.
MPEG4_SP_Encoder_S3_CIF.edf	CIF	Medium resolution core operating at CIF resolution for Spartan-3 device.
MPEG4_SP_Encoder_S3A_CIF.edf	CIF	Low Resolution Core operating at CIF resolution for a Spartan-3A device.
MPEG4_SP_Encoder_V4_4CIF.edf	4CIF	High resolution core operating at 4CIF resolution for a Virtex-4 device.
MPEG4_SP_Encoder_V5_4CIF.edf	4CIF	Low Resolution Core operating at 4CIF resolution for a Virtex-5 device.
MPEG4_SP_Encoder_V2P_4CIF.edf	4CIF	High resolution core operating at 4CIF resolution for a Virtex-II Pro device.
MPEG4_SP_Encoder_S3_4CIF.edf	4CIF	High-resolution core operating at 4CIF resolution for a Spartan-3 device.
MPEG4_SP_Encoder_S3A_4CIF.edf	4CIF	Low Resolution Core operating at 4CIF resolution for a Spartan-3A device.

Input Interface

This interface accepts data from the acquiring in 4:2:0 YUV macroblock format. The incoming data is 32- bits wide. The data is put into the encoder through a write enable while monitoring a full flag. If the user wants to send a burst of data to the encoder, an empty flag can be polled and a burst of data can be sent to the encoder if the empty state is detected.