OPB to OPB Bridge (Lite Version) (v1.00a)

DS475 December 2, 2005 Product Specification

Introduction

This document provides the design specification for the OPB to OPB Lite Bridge. The OPB to OPB Lite Bridge is used to connect two OPB buses. The bridge has one master port and one slave port. Two bridges may be used together to support full bus mastership in both directions.

Features

- Provides a bridge between two OPB V2.0 buses
- Connections for one master-side bus and one slave-side bus
- Parameterized data bus widths
- Simple transaction forwarding reduces LUT count
- Requires the two OPB buses to be on the same clock and the same size
- No support for data buffering or posted writes

Functional Description

The top level block diagram for the OPB to OPB Bridge Lite is shown in Figure 1. A transaction is initiated to the slave side of the bridge. The slave-side signals are registered in the slave attachment and the control state machine begins a request on the master side of the bridge. After the bus has been granted to the bridge, the master attachment begins a transaction on the master side, passing through the signals that were registered in the slave attachment. The transfer acknowledge signals, MOPB_xferAck, MOPB_errAck, MOPB_timeout, and MOPB entry, are passed back through the bridge to the slave side to complete the transaction. A time-out on the master side (MOPB_timeout asserted) is translated to an error acknowledge on the slave side (Sl_errAck asserted). No buffering for burst optimization is performed.

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	QPro™-R Virtex™-II, QPro Virtex-II, Spartan™-II, Spartan-IIE, Spartan-3, Spartan-3E, Virtex, Virtex-II, Virtex-II Pro, Virtex-4, Virtex-E	
Version of Core	opb_opb_lite	v1.00a
Resources Used		
	Min	Max
Slices	21	26
LUTs	22	30
FFs	27	27
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	5.1i or later	
Verification	N/A	
Simulation	ModelSim SE/EE 5.6e or later	
Synthesis	XST	
Support		
Support provided by Xilinx, Inc.		

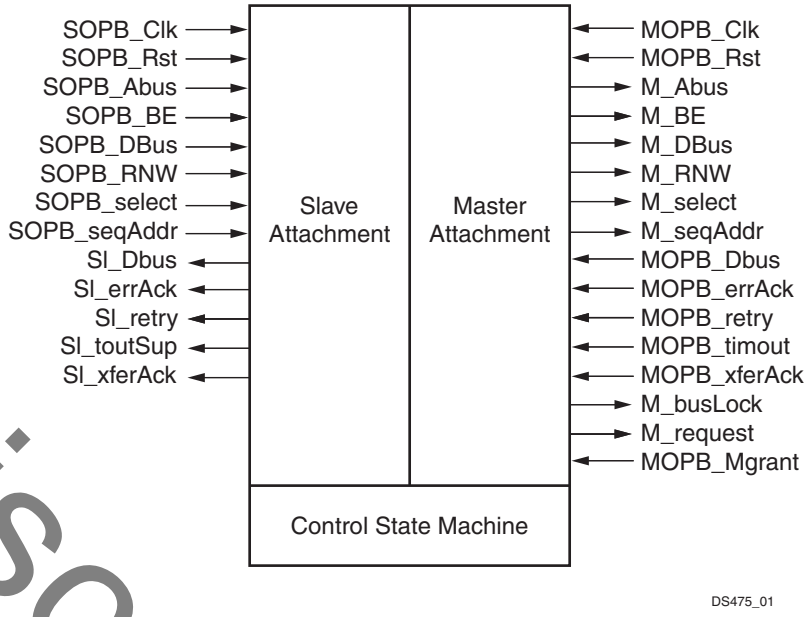

Figure 1: **OPB to OPB Lite Bridge Block Diagram**

Figure 2 shows a typical system with two OPB buses interconnected with a bridge. Any OPB master on OPB B can initiate a transaction (read or write) on OPB A. Note that masters on OPB A cannot get to OPB B unless another bridge is used in the opposite direction.

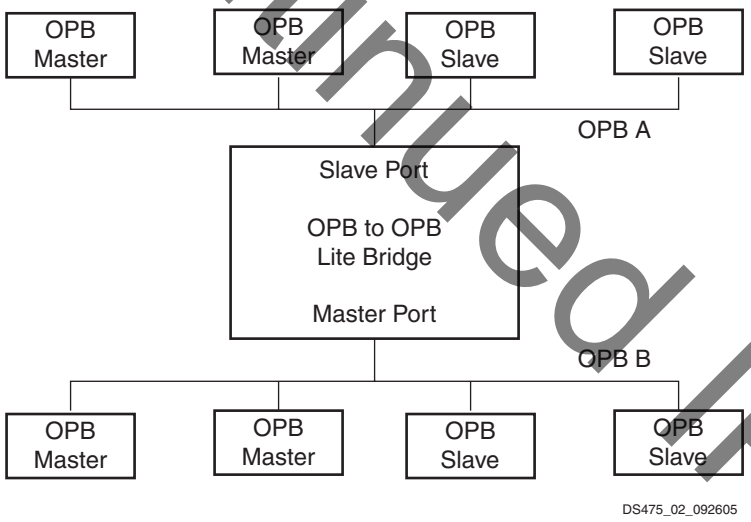

Figure 2: **OPB System with Bridge**

Figure 3 shows a system with two bridges. In this system, masters on OPB B can initiate reads and writes to slaves on OPB A, and masters on OPB A can initiate reads and writes to slaves on OPB B.

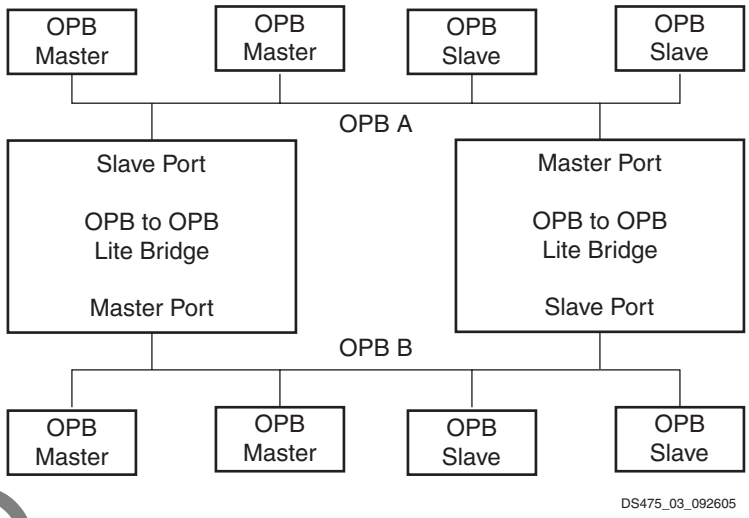

Figure 3: **OPB System with Two Lite Bridges**

OPB to OPB Lite Bridge I/O Signals

The I/O signals for the OPB to OPB Lite Bridge are listed in Table 1. The interfaces referenced in this table are shown in Figure 1 in the OPB to OPB Lite Bridge block diagram.

Table 1: **OPB to OPB Lite Bridge I/O Signals**

Signal Name	MSB:LSB	I/O	Description
Master-Side signals			
MOPB_Clk		I	OPB Clk (Master side)
MOPB_Rst		I	OPB Reset (Master side)
M_ABus	0:C_OPB_AWIDTH – 1	I	Master Address Bus
M_BE	0:C_OPB_DWIDTH/8 – 1	I	Master Byte Enables
M_busLock	0:C_NUM_MASTERS-1	I	Master Buslock
M_DBus	0:C_OPB_DWIDTH – 1	I	Master Databus
M_request		I	Master Request
M_RNW		I	Master Read/ Not Write
M_select		I	Master Select
M_seqAddr		I	Master Sequential Address
MOPB_DBus	0:C_OPB_DWIDTH – 1	O	OPB Data Bus
MOPB_errAck		O	OPB Error Acknowledge
MOPB_MGrant		O	OPB Master Grant
MOPB_retry		O	OPB Retry
MOPB_timeout		O	OPB Timeout
MOPB_xferAck		O	OPB Transfer Acknowledge

Table 1: **OPB to OPB Lite Bridge I/O Signals *(Contd)***

Signal Name	MSB:LSB	I/O	Description
Slave-Side signals			
SOPB_Clk		I	OPB Clk (Master side)
SOPB_Rst		I	OPB Reset (Master side)
SOPB_ABus	0:C_OPB_AWIDTH – 1	O	OPB Address Bus
SOPB_BE	0:C_OPB_DWIDTH/8 – 1	O	OPB Byte Enables
SOPB_DBus	0:C_OPB_DWIDTH – 1	O	OPB Data Bus
SOPB_RNW		O	OPB Read/ Not Write
SOPB_select		O	OPB Select
SOPB_seqAddr		O	OPB Sequential Address
SI_DBus	0:C_OPB_DWIDTH – 1	I	Slave Data Bus
SI_errAck		I	Slave Error Acknowledge
SI_retry		I	Slave Retry
SI_toutSup		I	Slave Timeout Suppress
SI_xferAck		I	Slave Transfer Acknowledge

OPB to OPB Lite Bridge Design Parameters

To obtain an OPB to OPB Bridge that is uniquely tailored to the user's system, certain features in the bridge can be parameterized. This allows for a high performance design that only utilizes the resources required by the system. The features that can be parameterized in the Xilinx OPB to OPB Bridge design are shown in Table 2.

Table 2: **OPB to OPB Lite Bridge Design Parameters**

Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Ty
Number of OPB Address Windows	C_NUM_DECODES	1 – 4	1	intege
OPB Data Bus Width	C_OPB_DWIDTH	8, 16, 32, 64, 128	32	intege
OPB Address Bus Width	C_OPB_AWIDTH	16 – 32	32	intege
Decode 0 Base Address	C_DEC0_BASEADDR	Valid Address Range(2)	None(1)	std_logic_v
Decode 0 High Address	C_DEC0_HIGHADDR		None(1)	std_logic_v
Decode 0 Base Address	C_DEC1_BASEADDR	Valid Address Range(2)	None(1)	std_logic_v
Decode 0 High Address	C_DEC1_HIGHADDR		None(1)	std_logic_v
Decode 0 Base Address	C_DEC2_BASEADDR	Valid Address Range(2)	None(1)	std_logic_v
Decode 0 High Address	C_DEC2_HIGHADDR		None(1)	std_logic_v

Table 2: **OPB to OPB Lite Bridge Design Parameters**

Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Ty
Decode 0 Base Address	C_DEC3_BASEADDR	Valid Address Range(2)	None(1)	std_logic_v
Decode 0 High Address	C_DEC3_HIGHADDR		None(1)	std_logic_v

Notes:

1. No default value will be specified for C_DECx_BASEADDR to insure that the actual value is set, i.e. if the value is not set, a c error will be generated.
2. Address range specified by C_DECx_BASEADDR and C_DECx_HIGHADDR must be at least 0x1 and must be a power of 2 = 2^n). The base address must start on a 2^n boundary (n LSBits of base address must equal 0).

Device Utilization

The following table shows the approximate resource utilization for the OPB to OPB Lite Bridge. The estimates shown are not guaranteed and can vary with FPGA family and speed grade, parameters selected for implementation, user timing constraints, and implementation tool version. Only parameters that affect resource utilization are shown in Table 3.

Table 3: **OPB to OPB Lite Bridge Resource Utilization (Virtex-II Pro)**

Parameter Values	Device Resources		
C_NUM_DECODES	Slices	Slice Flip-Flops	4-input LUTs
1	21	27	22
2	23	27	26
3	26	27	30
4	26	27	30

Reference Documents

The following documents contain reference information important to understanding the OPB Arbiter design:

- IBM 64-Bit On-Chip Peripheral Bus Architectural Specification (v2.0)
- OPB Usage in Xilinx FPGAs

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/29/02	1.0	Initial Xilinx release
11/11/02	1.1	Added Device Utilization table
01/07/03	1.2	Update copyright
07/07/03	1.3	Update to new template
07/29/03	1.3.1	Change DS254 to DS475 because of duplications
09/01/03	1.3.2	Update graphics to GSC standards and correct trademarks
12/12/03	1.3.3	Correct narrative for figure 1
8/6/04	1.3.4	Updated trademarks and supported family listing
9/26/05	1.4	Converted to new DS template; updated figures to Xilinx graphic standards.
12/2/05	1.5	Added Spartan-3E to supported device families listing.