Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/30/04	1.0	Initial Xilinx release.
11/11/04	1.1	Updated document with changes to performance numbers of the dynamic phase alignment configuration of the core.
04/28/05	1.2	Updated document to indicate support for Xilinx ISE Foundation v7.1i.
08/31/05	2.0	Added SP 3 to Xilinx ISE v7.1i, section about Global Clocking with DCM edited, various copy edits.
01/18/06	3.0	Updated ISE to v8.1i, revised dynamic alignment section.
07/13/06	4.0	Added support for Virtex-5, Updated ISE to v8.2i, release date.
09/21/06	4.1	Added new DPA-related signals. Updated for IP2i minor release.
02/15/07	4.2	Updated for IP1Jade release.
8/08/07	4.3	Updated for the IP1 Jade Minor release. Added SnkIdelayCtlRdy Input signal.
03/24/08	4.4	Modified description of ScerAFThresAssert[8:0] signal in Table 12, updated supported tools and core version.
09/19/08	4.5	Updated for the ISE service pack 3 release.
04/24/09	5.0	Updated core version to 9.1 and ISE to version 11.1. Added support for Virtex-6 devices.
06/24/09	5.5	Updated core version to 9.2 and ISE to version 11.2.
09/16/09	6.0	Updated core version to 9.3 and ISE to version 11.3. Added support for Virtex-6 -1L and Virtex-6 CXT devices.
04/22/10	7.0	Updated core version to 10.1 and ISE version to 12.1; added support for Spartan-6 devices.
09/21/10	8.0	Updated core version to 10.2 and ISE version to 12.3.
12/14/10	9.0	Updated core version to 10.3 and ISE version to 12.4; removed Spartan-6 support and updated Virtex-6 performance numbers and supported clocking scheme.
3/1/11	10.0	Updated core version to 10.4 and ISE version to 13.1.
6/22/11	11.0	Updated core version to 10.5 and ISE Design Suite version to 13.2.

Discontinued IP

Notice of Disclaimer

Xilinx is providing this product documentation, hereinafter "Information," to you "AS IS" with no warranty of any kind, express or implied. Xilinx makes no representation that the Information, or any particular implementation thereof, is free from any claims of infringement. You are responsible for obtaining any rights you may require for any implementation based on the Information. All specifications are subject to change without notice. XILINX EXPRESSLY DISCLAIMS ANY WARRANTY WHATSOEVER WITH RESPECT TO THE ADEQUACY OF THE INFORMATION OR ANY IMPLEMENTATION BASED THEREON, INCLUDING BUT NOT LIMITED TO ANY WARRANTIES OR REPRESENTATIONS THAT THIS IMPLEMENTATION IS FREE FROM CLAIMS OF INFRINGEMENT AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Except as stated herein, none of the Information may be copied, reproduced, distributed, republished, downloaded, displayed, posted, or transmitted in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx.