PLBV46 Master Single (v1.00a)

DS563 April 24, 2009 **Product Specification**

Introduction

The PLBV46 Master Single is a continuation of the Xilinx family of IBM CoreConnect compatible LogiCORE products. It provides a bi-directional interface between a User IP core and the PLB v4.6 bus standard. This version of the PLBV46 Master Single has been optimized for Master operations consisting of single data beat read or write transfers of 1 to 4 bytes.

Features

- Compatible with IBM CoreConnect 32, 64 and 128-bit PLB.
- Resource optimize design
  - 32-bit internal native data width.
  - Supports single beat read and write data transfers of up to 4 bytes (32-bits)

LogiCORE™ IP Facts		
Core Specifics		
See EDK Supported Device Families.		
Version of Core	lmb_v10	v2.00a
Resources Used		
	Min	Max
Slices	N/A	N/A
LUTs	0	353
FFs	0	0
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	See Tools for requirements.	
Verification		
Simulation		
Synthesis		
Support		
Provided by Xilinx, Inc.		

Functional Description

The PLBV46 Master Single is designed to provide a user with a quick way to implement light weight mastering interface between user logic and the IBM PLB. Figure 1 shows a block diagram of the PLBV46 Master Single. The port references and groupings are detailed in Table 1. The design is natively 32-bits and supports read and write transfers of 1 to 4 bytes. Transfer request protocol between the PLB and the User Logic is provided by the Read and Write Controller block. The Bus Width Adapter and Steering Logic block provides the necessary function to connect a 32-bit Master to the three available PLB widths; 32, 64, and 128-bits. The PLB attachment width is set via VHDL parameterization.

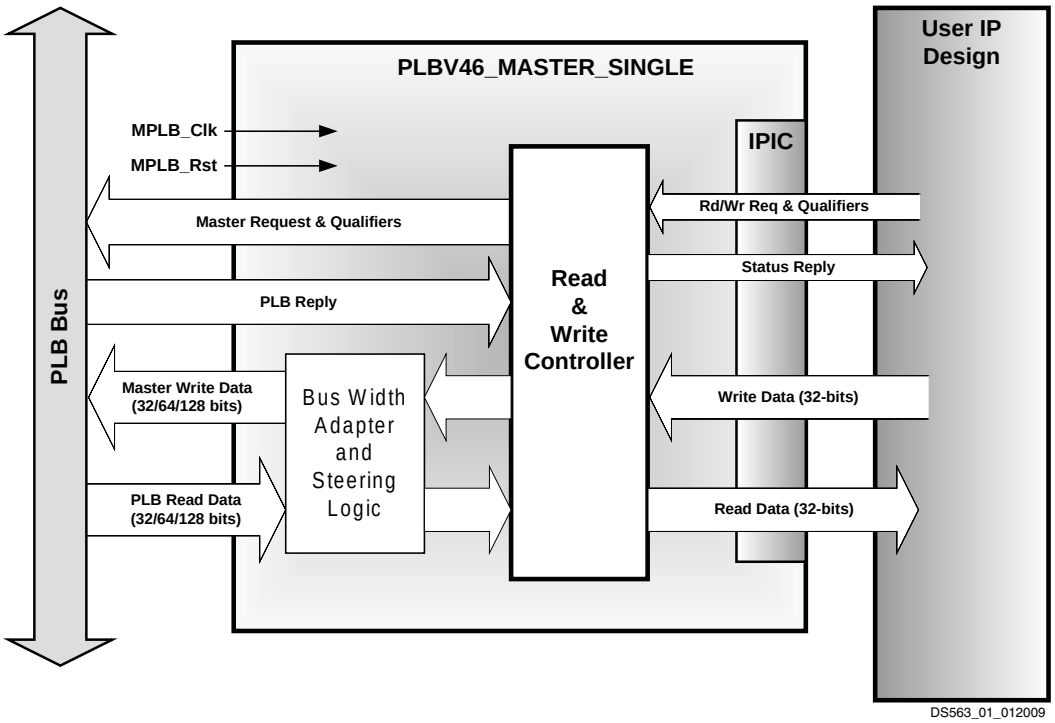

Figure 1: **PLBV46 Master Single Block Diagram**

I/O Signals

The PLBV46 Master Single signals are listed and described in Table 1.

Table 1: **PLBV46 Master Single I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
PLB Clock and Reset				
MPLB_Clk	PLB Bus	I		PLB main bus clock. See table note 1.
MPLB_Rst	PLB Bus	I		PLB main bus reset. See table note 1..
Other System Signal				
MD_error	PLB Bus	O	'0'	Master Detected Error Status Output
PLB Request and Qualifier Signals				
M_request	PLB Bus	O	'0'	See table note 1.
M_priority	PLB Bus	O	'0'	
M_buslock	PLB Bus	O	'0'	
M_RNW	PLB Bus	O	'0'	
M_BE(0:[**C_MPLB_DWIDTH**/8] -1)	PLB Bus	O	zeros	
M_Msize(0:1)	PLB Bus	O	"00"	
M_size(0:3)	PLB Bus	O	"0000"	
M_type(0:2)	PLB Bus	O	"000"	
M_ABus(0:**31**)	PLB Bus	O	zeros	
M_wrDBus(0:**C_MPLB_DWIDTH**-1)	PLB Bus	O	zeros	
PLB Reply Signals				
PLB_MaddrAck	PLB Bus	I		See table note 1.
PLB_Mrearbitrate	PLB Bus	I		
PLB_MTimeout	PLB Bus	I		
PLB_MRdErr	PLB Bus	I		
PLB_MWrErr	PLB Bus	I		
PLB_MRdDBus(0:**C_MPLB_DWIDTH**-1)	PLB Bus	I		
PLB_MRdDAck	PLB Bus	I		
PLB_MWrDAck	PLB Bus	I		
PLB Signal Ports Included in the Design but Unused Internally				

Table 1: **PLBV46 Master Single I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
M_TAttribute(0 to 15)	PLB Bus	O	’0’	
M_lockerr	PLB Bus	O	’0’	
M_abort	PLB Bus	O	’0’	
M_UABus(0:**31)**)	PLB Bus	O	zeros	
M_wrBurst	PLB Bus	O	’0’	
M_rdBurst	PLB Bus	O	’0’	
PLB_MSSize(0:1)	PLB Bus	I		See table note 2.
PLB_MBusy	PLB Bus	I		
PLB_MIRQ	PLB Bus	I		
PLB_RdWdAddr(0:3)	PLB Bus	I		
PLB_RdBTerm	PLB Bus	I		
PLB_MWrBTerm	PLB Bus	I		
IPIC Command Interface Signals				
IP2Bus_MstRd_Req	IPIC	I		User Logic Read Request
IP2Bus_MstWr_Req	IPIC	I		User Logic Write Request
IP2Bus_Mst_Addr(0 to C_MPLB_AWIDTH-1)	IPIC	I		User Logic Request Address
IP2Bus_Mst_BE(0 to C_MPLB_NATIVE_DWIDTH-1)	IPIC	I		User Logic Request Byte Enables
IP2Bus_Mst_Lock	IPIC	I		Reserved: Tie to Logic low. User Logic Bus Lock Request.
IP2Bus_Mst_Reset	IPIC	I		Optional User Logic Reset Request.
Bus2IP_Mst_CmdAck	IPIC	O	’0’	Command Acknowledge Status
Bus2IP_Mst_Cmplt	IPIC	O	’0’	Command Complete Status
Bus2IP_Mst_Error	IPIC	O	’0’	Command Error Status
Bus2IP_Mst_Rearbitrate	IPIC	O	’0’	Command Rearbitrate Status
Bus2IP_Mst_Timeout	IPIC	O	’0’	Command Timeout Status

Table 1: **PLBV46 Master Single I/O Signal Description**

Signal Name	Interface	Signal Type	Init Status	Description
IPIC Read Data Interface Signals				
Bus2IP_MstRd_d(0 to C_MSPLB_NATIVE_DWIDTH-1)	IPIC	O	zeros	Read data output to User Logic
Bus2IP_MstRd_src_rdy_n	IPIC	O	'1'	Active low signal indicating that the data value asserted on the Bus2IP_MstRd_d Bus is valid
IPIC Read Data Interface Signals				
IP2Bus_MstWr_d(0 to C_MSPLB_NATIVE_DWIDTH-1)	IPIC	I		Write data input from the User Logic
IP2Bus_MstWr_dst_rdy_n	IPIC	O	'1'	Active low signal indicating that the data value asserted on the IP2Bus_MstWr_d Bus is has been transferred on the PLB

Note:

1. This signal's function and timing is defined in the IBM **128-Bit Processor Local Bus Architecture Specification Version 4.6.**
2. Output ports that are not used are driven to constant logic levels that are consistent with the inactive state for the subject signal. Input ports that are required but not used are internally ignored by the design.

Design Parameters

The PLBV46 Master Single provides for User interface tailoring via VHDL Generic parameters. These parameters are detailed in Table 2..

Table 2: **PLBV46 Master Single Design Parameters**

Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type
PLB I/O Specification				
Specifies the Number of Used Address bits out of the available 64 bits of PLBV46 addressing	C_MPLB_AWIDTH	32	32	integer
Width of the PLB Data Bus to which the Master is attached	C_MPLB_DWIDTH	32, 64, 128	32	integer
Specifies the internal native data width of the Master	C_MPLB_NATIVE_DWIDTH	32	32	integer
FPGA Family Type				
Xilinx FPGA Family	C_FAMILY	See C_FAMILY parameter values.		string

Allowable Parameter Combinations

Parameter - Port Dependencies

Table 3: **PLBV46 Master Single Parameter-Port Dependencies**

Name (Generic or Port)	Affects (Port)	Depends (Generic)	Relationship Description
Design Parameters			
C_MPLB_AWIDTH	IP2Bus_Mst_Addr		The Parameter directly sets the ports width
C_MPLB_DWIDTH	M_BE		The BE Bus width is derived from the parameter value by dividing it by 8
C_MPLB_DWIDTH	M_wrDBus		The port width is directly set by the parameter value
C_MPLB_DWIDTH	PLB_MRdDBus		The port width is directly set by the parameter value

Table 3: **PLBV46 Master Single Parameter-Port Dependencies**

Name (Generic or Port)	Affects (Port)	Depends (Generic)	Relationship Description
C_MPLB_NATIVE_DWIDTH	IP2Bus_Mst_BE		The IPIC BE Bus width is derived from the parameter value by dividing it by 8
C_MPLB_NATIVE_DWIDTH	Bus2IP_Mst Rd_d		The IPIC Read Data port width is directly set by the parameter value
C_MPLB_NATIVE_DWIDTH	IP2Bus_Mst Wr_d		The IPIC Write Data port width is directly set by the parameter value

Parameter Detailed Descriptions

C_MPLB_AWIDTH

This integer parameter is used by the PLBV46 Master Single to size internal address related components and the input address from the User logic on the Command Interface. The parameter is provided for future growth beyond 32-bit addressing. Currently, the parameter value is only allowed to be set 32.

C_MPLB_DWIDTH

This integer parameter is used by the PLBV46 Master Single to size and optimize the PLBV46 data bus interface logic. This value should be set to match the actual width of the PLBV46 bus, 32, 64 or 128-Bits.

C_MPLB_NATIVE_DWIDTH

This integer parameter is used to specify the internal data width of the PLBV46 Master Single as well as the IPIC data width to the User Logic. The parameter is provided for future growth beyond 32-bit data widths with User logic. Currently, the parameter value is only allowed to be set 32.

C_FAMILY

This parameter is defined as a string. It specifies the target FPGA technology for implementation of the PLB Slave. This parameter is required for proper selection of FPGA primitives. Currently, the PLBV46 Master Single does not implement any FPGA primitives that require the use of this parameter.

IPIC Transaction Timing

The following section shows timing relationships for PLBV46 and IPIC interface signals during read and write transfers. Only single data beat transfers of 1 to 4 bytes are supported by this Master.

Single Data Beat Read Operation

Two single beat read cycles are shown in Figure 2. The first cycle shows the PLB Slave address and data acknowledging the read cycle at the earliest allowed times by the PLB specification. The second read transfer indicates a more typical address acknowledge sequence and a delayed read data acknowledge by the PLB Slave device.

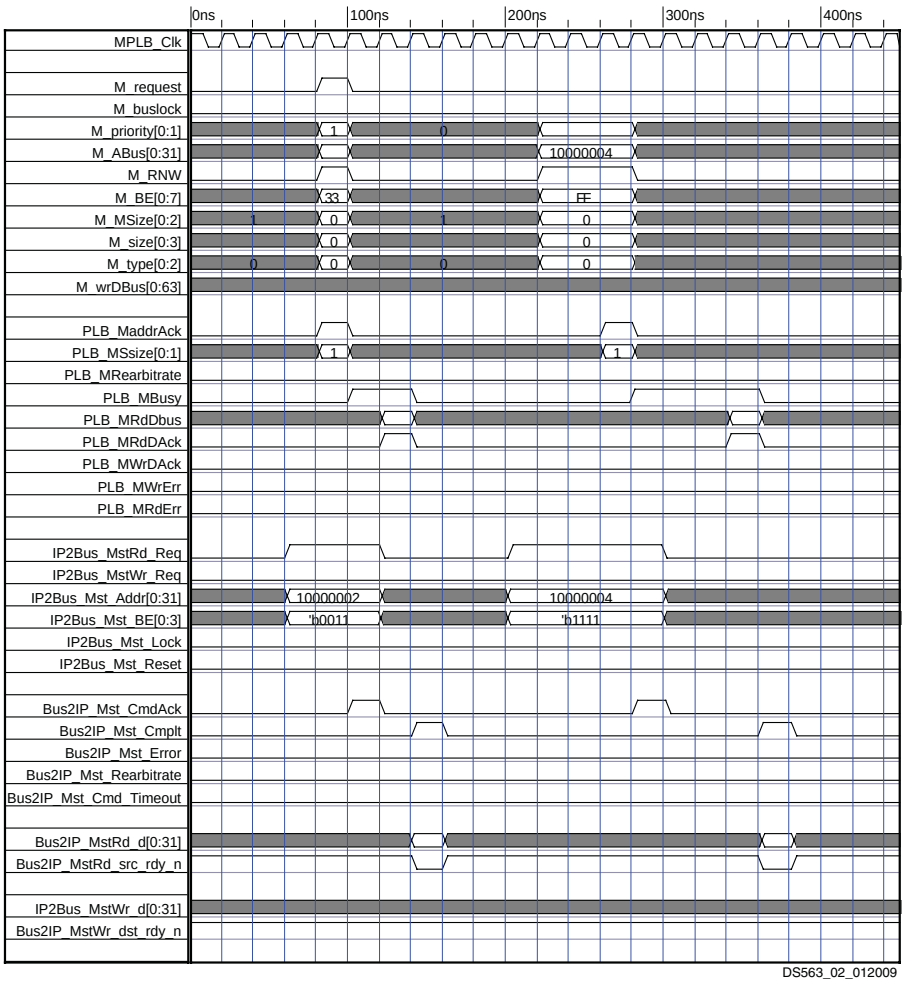

Figure 2: **PLB Single Data Beat Read Timing**

Single Data Beat Write Operation

Two single beat write cycles are shown in Figure 3. The first cycle shows the PLB Slave address and data acknowledging the write cycle at the earliest allowed times by the PLB specification. The second, write transfer indicates a more typical address acknowledge sequence and a delayed write data acknowledge by the PLB Slave device.

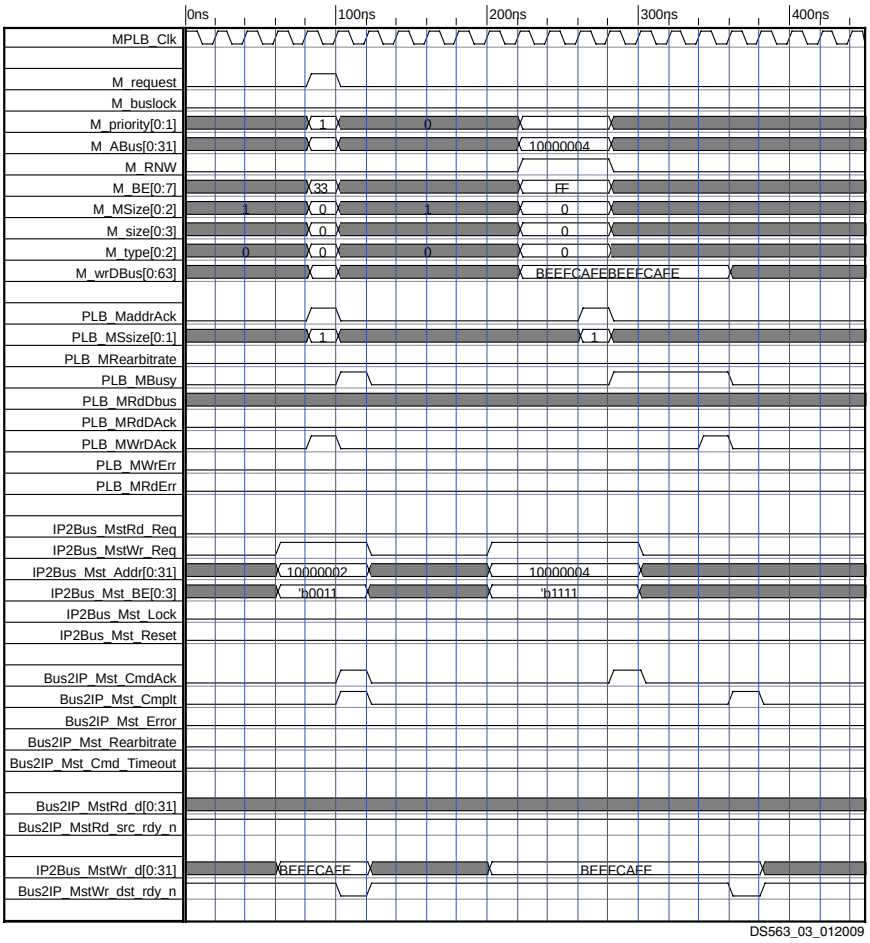

Figure 3: **PLB Single Data Beat Write Timing**

Single Data Beat Read With Error

Single data beat Read transfers with a Slave reported error is shown in Figure 4. For both transfers a Slave data error is reported and the Master's MD_Error output is asserted and held. The first assertion of MD_Error is cleared by the IP2Bus_Mst_Reset input from the IPIC interface. The second assertion of MD_Error is cleared by the MPLB_Rst input from the PLBV46 interface.

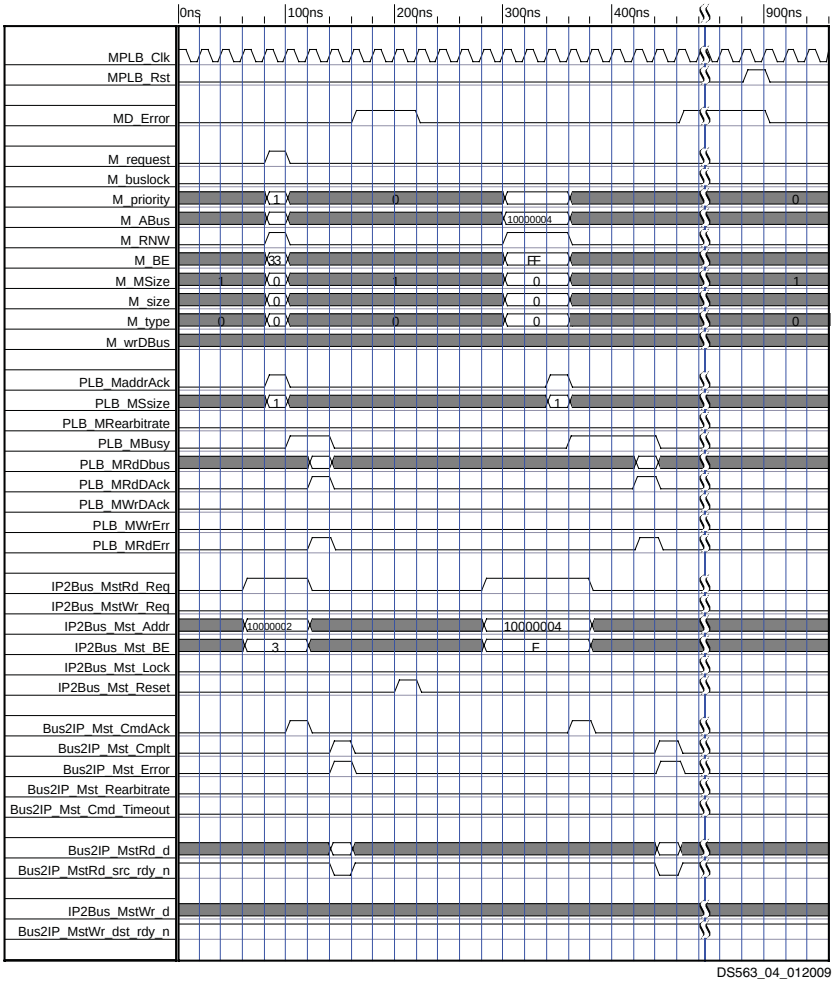

Figure 4: **PLB Single Data Beat Read Error Timing**

Single Data Beat Write With Error

Two single beat write cycles are shown in Figure 5. For both transfers, a Slave data error is reported and the Master's MD_Error output is asserted and held. The first assertion of MD_Error is cleared by the IP2Bus_Mst_Reset input from the IPIC interface. The second assertion of MD_Error is cleared by the MPLB_Rst input from the PLBV46 interface.

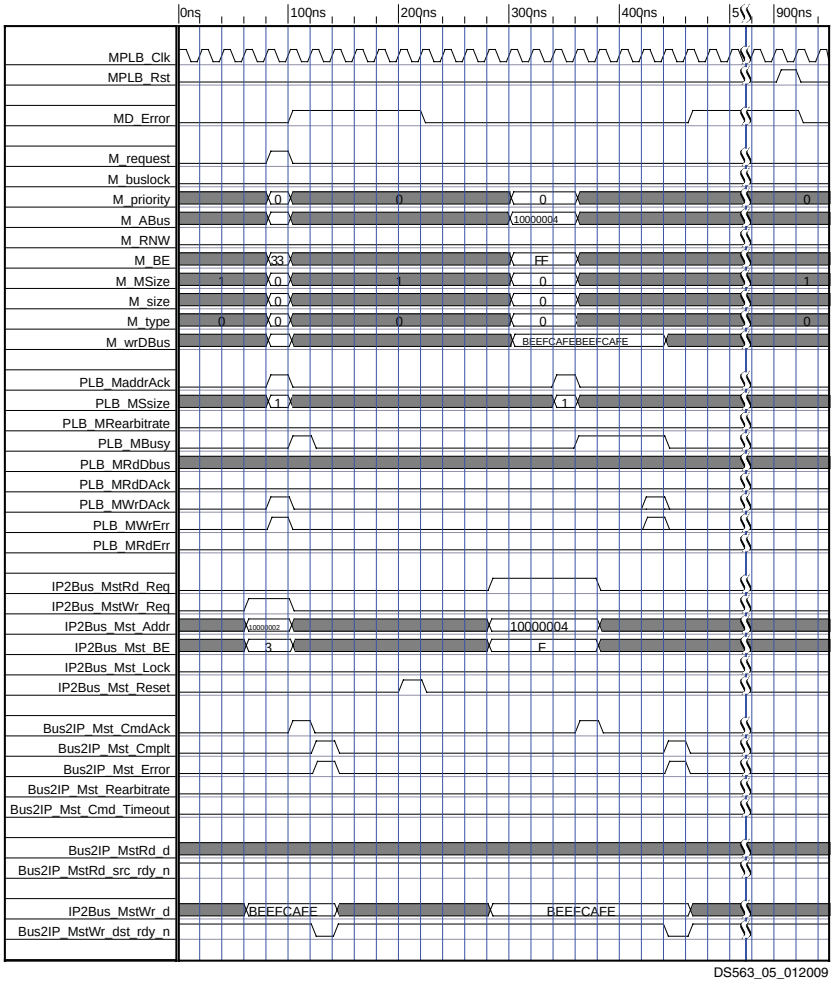

Figure 5: **PLB Single Data Beat Write Error Timing**

Address Phase Timeout

An attempted single data beat read operation that results in an Address Phase timeout is shown in Figure 6. The Master's MD_Error output is asserted and held upon detection of the PLB_MTimeout assertion. The Master's request, address, and qualifiers are removed from the PLB on the following PLB clock after the timeout indication and a timeout status is relayed to the User logic on the IPIC. For this example, the assertion of MD_Error is cleared by the MPLB_Rst input from the PLBV46 interface.

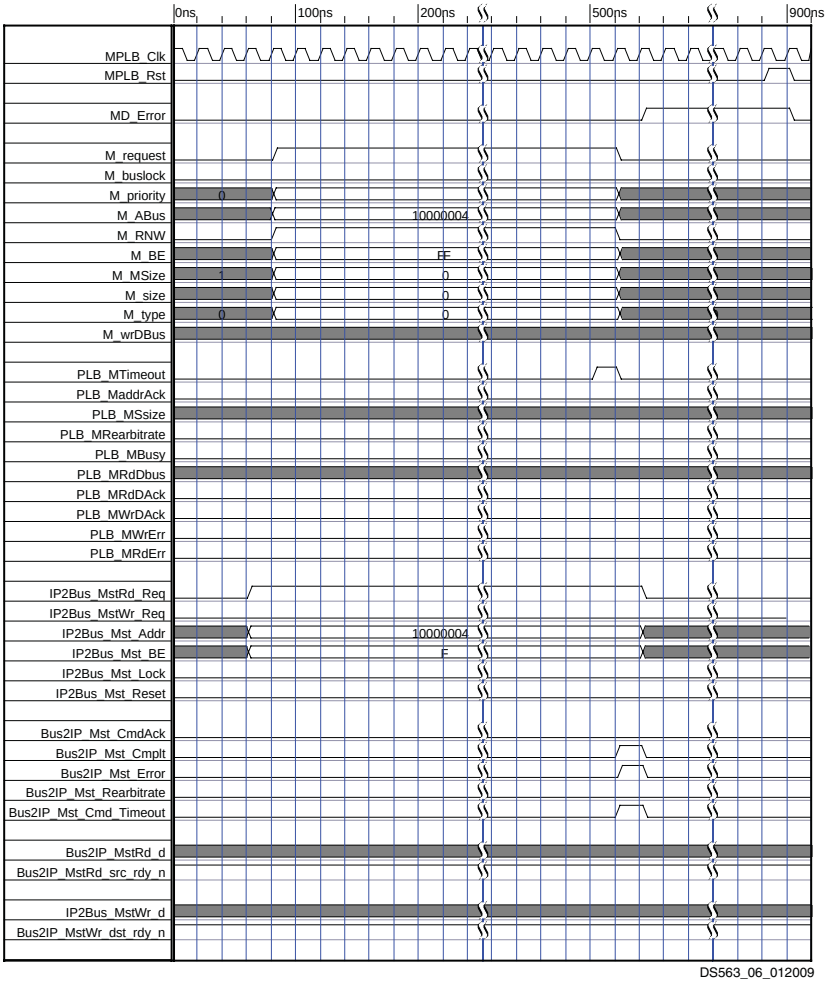

Figure 6: **PLB Address Phase Timeout Timing**

Register Descriptions

The PLBV46 Master Single has no User accessible registers.

Design Implementation

Target Technology

The target technology is an FPGA listed in EDK Supported Device Families.

Device Utilization and Performance Benchmarks

Since the PLBV46 Master Single is a module that will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section should be considered engineering estimates. As the PLBV46 Master Single is combined with other pieces of the User FPGA design, the utilization of FPGA resources and timing will vary from the results reported here.

The resource utilization of this version of the PLBV46 Master Single is shown in Table 4 for currently changeable parameter configurations. The design resource utilization numbers are taken from the resource utilization section of the Xilinx ISE® MAP report that is created by the MAP tool.

The PLBV46 Master Single benchmarks are shown in Table 4 for a Virtex-4 -10 FPGA.

Table 4: **Performance and Resource Utilization Benchmark**

Parameter Values(1)	Device Resources			F_{MAX}(2)
C_MPLB_DWIDTH	Slices	Slice Flip-Flops	4-input LUTs	F_{MAX}(2)
32	67	112	8	>200 MHz
64	67	112	8	>200 MHz
128	67	112	8	>200 MHz

Notes:

1. C_MPLB_AWIDTH fixed at 32 and C_MPLB_NATIVE_DWIDTH fixed at 32. The setting of C_FAMILY currently does not effect design resources.
2. F_{MAX} represents the maximum frequency of the PLBV46 Master Single in a standalone configuration. The actual maximum frequency will depend on the entire system and may be greater or less than what is recorded in this table.

Specification Exceptions

The following High Level PLB features are **not** supported by the PLBV46 Master Single design.

- Bus Slave
- Split Bus Transactions
- Address Pipelining
- Command Abort
- Fixed Length Burst
- Indeterminate Length Burst
- Cacheline

Reference Documents

The following documents contain reference information important to understanding the PLBV46 Master Single design.

1. IBM CoreConnect128-Bit Processor Local Bus, Architectural Specification (v4.6)
2. SP026 PLBV46 Interface Simplifications

Revision History

Date	Version	Revision
7/20/07	1.0	Initial XIlinx Release
4/21/08	1.1	Added Automotive Spartan-3E, Automotive Spartan-3A, Automotive Spartan-3, and Automotive Spartan-3A DSP support.
4/24/09	1.2	Replaced references to supported device families and tool name(s) with hyperlink to PDF file.

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