Introduction

The Phase Locked Loop primitive in Virtex-5 and Spartan-6 parts is used to generate multiple clocks with defined phase and frequency relationships to a given input clock. The Phase Locked Loop (PLL) module is a wrapper around the PLL_ADV primitive that allows the PLL to be used in the EDK tool suite.

Features

- Wrapper around the PLL_ADV primitive
- Full support for use with EDK 11.1 and later versions
- Configurable BUFG insertion
- Configurable output delay adjustment for PPC block clock insertion delay compensation in Virtex-5 FXT parts
- Six output clocks with independently selectable frequencies

| LogiCORE™ Facts |
| Core Specifics |
| Supported Device Family | Virtex®, Spartan®-6 |
| Resources Used | I/O | LUTs | FFs | Block RAMs |
| | N/A | N/A | N/A | N/A |
| Special Features | 1 PLL Block |

| Provided with Core |
| Documentation | Product Specification |
| Design File Formats | VHDL |
| Constraints File | N/A |
| Verification | N/A |
| Instantiation Template | N/A |
| Additional Items | None |

| Design Tool Requirements |
| Xilinx Implementation Tools | ISE® 11.1 or later |
| Verification | N/A |
| Simulation | N/A |
| Synthesis | N/A |

Support

Provided by Xilinx, Inc.
Functional Description

The PLL Module takes an input clock named CLKIN1, then generates several output clocks, each of which can be configured to have a different frequency that is dependent on the input clock frequency. The PLL Module encapsulates the PLL_ADV primitive as shown in Figure 1. The PLL_ADV primitive is described in the Libraries Guide for the applicable family that is provided as part of the ISE tools documentation.

The PLL Module provides optional buffers for the CLKIN1 input, and the CLKOUT*, and CLKFBOUT outputs. CLKOUT* represents the six clock outputs CLKOUT0, CLKOUT1, CLKOUT2, CLKOUT3, CLKOUT4, and CLKOUT5. The second clock input of the PLL_ADV primitive is not used, and the clock input select input of the PLL_ADV primitive is connected to a constant to always select the CLKIN1 signal. The dynamic reconfiguration inputs and outputs of the PLL_ADV primitive are hidden or terminated within the PLL module, as is the control input for the PMCD mode. All other inputs and outputs of the PLL_ADV primitive are inputs and outputs of the PLL module.

![Figure 1: PLL Module Implementation and Usage](image)

In the context of an embedded processor system, the recommended usage of the PLL module is to take a single reference clock input, then configure the CLKOUT* signals to produce the different clock frequencies and phases required, with the CLKOUT* and CLKFBOUT signals buffered and connected as shown by the dashed lines in Figure 1.

The output clock frequencies are derived from the input clock frequency, and the values of the following parameters: C_DIVCLK_DIVIDE, C_CLKFBOUT_MULT, C_CLKOUTn_DIVIDE.

\[
\text{Frequency of } \text{CLKOUTn} = \text{Frequency of } \text{CLKIN1} \times \left(\frac{\text{C_CLKFBOUT_MULT}}{\text{C_DIVCLK_DIVIDE}}\right) / \text{C_CLKOUTn_DIVIDE}
\]
PLL Module Parameters

The PLL module is configured by selecting appropriate values for the MPD (Microprocessor Peripheral Definition) parameters described in Table 1.

Table 1: MPD Parameters for PLL Module

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Allowed Values</th>
<th>Default Value</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_BANDWIDTH</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>OPTIMIZED</td>
<td>string</td>
</tr>
<tr>
<td>C_CLKFBOUT_BUF</td>
<td>If C_CLKFBOUT_BUF = true, a BUFG is inserted between the CLKFBOUT primitive and CLKFBOUT output</td>
<td>true, false</td>
<td>false</td>
<td>Boolean</td>
</tr>
<tr>
<td>C_CLKFBOUT_DESKEW_ADJUST</td>
<td>Clock delay attribute for CLKOUT5 output</td>
<td>NONE, PPC(1)</td>
<td>NONE</td>
<td>string</td>
</tr>
<tr>
<td>C_CLKFBOUT_MULT</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>1</td>
<td>integer</td>
</tr>
<tr>
<td>C_CLKFBOUT_PHASE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.0</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKIN1_BUF</td>
<td>If C_CLKIN1_BUF = true, a BUFG is inserted between the CLKIN1 input and the CLKIN1 pin of the PLL_ADV primitive</td>
<td>true, false</td>
<td>false</td>
<td>Boolean</td>
</tr>
<tr>
<td>C_CLKIN1_PERIOD</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.0</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT0_BUF</td>
<td>If C_CLKOUT0_BUF = true, a BUFG is inserted between the CLKOUT0 output</td>
<td>true, false</td>
<td>false</td>
<td>Boolean</td>
</tr>
<tr>
<td>C_CLKOUT0_DESKEW_ADJUST</td>
<td>Clock delay attribute for CLKOUT0 output</td>
<td>NONE, PPC(1)</td>
<td>NONE</td>
<td>string</td>
</tr>
<tr>
<td>C_CLKOUT0_DIVIDE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>1</td>
<td>integer</td>
</tr>
<tr>
<td>C_CLKOUT0_DUTY_CYCLE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.5</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT0_PHASE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.0</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT1_BUF</td>
<td>If C_CLKOUT1_BUF = true, a BUFG is inserted between the CLKOUT1 output</td>
<td>true, false</td>
<td>false</td>
<td>Boolean</td>
</tr>
<tr>
<td>C_CLKOUT1_DESKEW_ADJUST</td>
<td>Clock delay attribute for CLKOUT1 output</td>
<td>NONE, PPC(1)</td>
<td>NONE</td>
<td>string</td>
</tr>
</tbody>
</table>
### Table 1: MPD Parameters for PLL Module (Cont’d)

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Allowed Values</th>
<th>Default Value</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_CLKOUT1_DIVIDE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>1</td>
<td>integer</td>
</tr>
<tr>
<td>C_CLKOUT1_DUTY_CYCLE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.5</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT1_PHASE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.0</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT2_BUF</td>
<td>If C_CLKOUT2_BUF = true, a BUFG is inserted between the CLKOUT2 pin of the PLL_ADV primitive and CLKOUT2 output</td>
<td>true, false</td>
<td>false</td>
<td>Boolean</td>
</tr>
<tr>
<td>C_CLKOUT2_DUTY_CYCLE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.5</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT2_PHASE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.0</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT2_ADMIN</td>
<td>Clock delay attribute for CLKOUT2 output</td>
<td>NONE, PPC(1)</td>
<td>NONE</td>
<td>string</td>
</tr>
<tr>
<td>C_CLKOUT2_DIVIDE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>1</td>
<td>integer</td>
</tr>
<tr>
<td>C_CLKOUT2_DUTY_CYCLE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.5</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT3_BUF</td>
<td>If C_CLKOUT3_BUF = true, a BUFG is inserted between the CLKOUT3 pin of the PLL_ADV primitive and CLKOUT3 output</td>
<td>true, false</td>
<td>false</td>
<td>Boolean</td>
</tr>
<tr>
<td>C_CLKOUT3_DUTY_CYCLE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.5</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT3_ADMIN</td>
<td>Clock delay attribute for CLKOUT3 output</td>
<td>NONE, PPC(1)</td>
<td>NONE</td>
<td>string</td>
</tr>
<tr>
<td>C_CLKOUT3_DIVIDE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>1</td>
<td>integer</td>
</tr>
<tr>
<td>C_CLKOUT3_DUTY_CYCLE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.5</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT3_PHASE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.0</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT4_BUF</td>
<td>If C_CLKOUT4_BUF = true, a BUFG is inserted between the CLKOUT4 pin of the PLL_ADV primitive and CLKOUT4 output</td>
<td>true, false</td>
<td>false</td>
<td>Boolean</td>
</tr>
<tr>
<td>C_CLKOUT4_DUTY_CYCLE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.5</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT4_ADMIN</td>
<td>Clock delay attribute for CLKOUT4 output</td>
<td>NONE, PPC(1)</td>
<td>NONE</td>
<td>string</td>
</tr>
<tr>
<td>C_CLKOUT4_DIVIDE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>1</td>
<td>integer</td>
</tr>
</tbody>
</table>
### Table 1: MPD Parameters for PLL Module (Cont’d)

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Allowed Values</th>
<th>Default Value</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_CLKOUT4_DUTY_CYCLE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.5</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT4_PHASE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.0</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT5_BUF</td>
<td>If C_CLKOUT5_BUF = true, a BUFG is inserted between the CLKOUT5 pin of the PLL_ADV primitive and CLKOUT5 output</td>
<td>true, false</td>
<td>false</td>
<td>Boolean</td>
</tr>
<tr>
<td>C_CLKOUT5_DESKEW_ADJUST</td>
<td>Clock delay attribute for CLKOUT5 output</td>
<td>NONE, PPC(1)</td>
<td>NONE</td>
<td>string</td>
</tr>
<tr>
<td>C_CLKOUT5_DIVIDE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>1</td>
<td>integer</td>
</tr>
<tr>
<td>C_CLKOUT5_DUTY_CYCLE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.5</td>
<td>real</td>
</tr>
<tr>
<td>C_CLKOUT5_PHASE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.0</td>
<td>real</td>
</tr>
<tr>
<td>C_COMPENSATION</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>SYSTEM_SYNCHRONOUS</td>
<td>string</td>
</tr>
<tr>
<td>C_DIVCLK_DIVIDE</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>1</td>
<td>integer</td>
</tr>
<tr>
<td>C_EXT_RESET_HIGH</td>
<td>IF C_EXT_RESET_HIGH = 0, the RST signal is inverted before connecting to the PLL_ADV</td>
<td>0,1</td>
<td>1</td>
<td>integer</td>
</tr>
<tr>
<td>C_FAMILY</td>
<td>Target FPGA family</td>
<td>virtex5, virtex5fx, spartan6, spartan6t</td>
<td>NONE</td>
<td>string</td>
</tr>
<tr>
<td>C_REF_JITTER</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>0.1</td>
<td>real</td>
</tr>
<tr>
<td>C_RESET_ON_LOSS_OF_LOCK</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>false</td>
<td>Boolean</td>
</tr>
<tr>
<td>C_RST_DEASSERT_CLK</td>
<td>This parameter passes the value to the equivalent attribute of the PLL_ADV</td>
<td>Same as PLL_ADV</td>
<td>CLKIN1</td>
<td>string</td>
</tr>
</tbody>
</table>

**Notes:**
1. The C_CLKOUTn_DESKEW_ADJUST value “PPC” applies only to Virtex-5 FXT designs.
Allowable Parameter Combinations

The C_CLKOUTn_DESKEW_ADJUST parameter must be set to NONE for clock outputs connected to the CPMC440CLK and CPMINTERCONNECTCLK pins on the ppc440 primitive in Virtex-5 FXT. Clock output signals connected to any other pins on the ppc440 primitive must have the C_CLKOUTn_DESKEW_ADJUST parameter set to PPC. Clock output signals connected to soft logic modules that connect to the ppc440 primitive must have the C_CLKOUTn_DESKEW_ADJUST parameter set to PPC. For Virtex-5 FXT designs, the C_CLKFBOUT_BUF parameter must be set to true when used in the recommended configuration shown in Figure 1. For Virtex-5 FXT designs, the C_CLKOUTn_BUF parameters must be set to true for any clock output that is used. The PLL_ADV primitive has additional restrictions on parameter combinations that are allowed for Virtex-5 FXT designs. The restrictions are documented in the Virtex-5 User Guide and Virtex-5 Libraries Guide.

Note: The PLL Module wrapper does not perform any error checking to enforce the design rules and restrictions described in the Virtex-5 User Guide.

PLL Module I/O Signals

The input and output signals of the PLL module are described in Table 2.

The table below contains an example of how to create cross-references from the table body to the table notes.

Table 2: PLL Module Input and Output Signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKFBDCM</td>
<td>Output</td>
<td>Feedback clock signal to use when the PLL drives a DCM or is driven by a DCM</td>
</tr>
<tr>
<td>CLKFBOUT</td>
<td>Output</td>
<td>Feedback clock output to be connected to CLKFBIN</td>
</tr>
<tr>
<td>CLKOUT0</td>
<td>Output</td>
<td>Clock output 0</td>
</tr>
<tr>
<td>CLKOUT1</td>
<td>Output</td>
<td>Clock output 1</td>
</tr>
<tr>
<td>CLKOUT2</td>
<td>Output</td>
<td>Clock output 2</td>
</tr>
<tr>
<td>CLKOUT3</td>
<td>Output</td>
<td>Clock output 3</td>
</tr>
<tr>
<td>CLKOUT4</td>
<td>Output</td>
<td>Clock output 4</td>
</tr>
<tr>
<td>CLKOUT5</td>
<td>Output</td>
<td>Clock output 5</td>
</tr>
<tr>
<td>CLKOUTDCM0</td>
<td>Output</td>
<td>Local copy of CLKOUT0 that connects to the DCM within the same tile</td>
</tr>
<tr>
<td>CLKOUTDCM1</td>
<td>Output</td>
<td>Local copy of CLKOUT1 that connects to the DCM within the same tile</td>
</tr>
<tr>
<td>CLKOUTDCM2</td>
<td>Output</td>
<td>Local copy of CLKOUT2 that connects to the DCM within the same tile</td>
</tr>
<tr>
<td>CLKOUTDCM3</td>
<td>Output</td>
<td>Local copy of CLKOUT3 that connects to the DCM within the same tile</td>
</tr>
<tr>
<td>CLKOUTDCM4</td>
<td>Output</td>
<td>Local copy of CLKOUT4 that connects to the DCM within the same tile</td>
</tr>
<tr>
<td>CLKOUTDCM5</td>
<td>Output</td>
<td>Local copy of CLKOUT5 that connects to the DCM within the same tile</td>
</tr>
<tr>
<td>LOCKED</td>
<td>Output</td>
<td>Synchronous output that goes high when the PLL has achieved phase alignment and frequency matching</td>
</tr>
</tbody>
</table>
### Register Descriptions
Not Applicable.

### Timing Diagrams
See the Virtex-5 User Guide for more information.

### Design Implementation

#### Target Technology
This module is intended for use on Spartan-6 and Virtex-5 FXT devices (the PLL_ADV primitive is available on all Virtex-5 devices).

#### Device Utilization and Performance Benchmarks
This module uses one PLL primitive and one BUFG primitive for each clock output that is used.

### Reference Documents
1. [UG190 Virtex-5 User Guide](#)
2. [Virtex-5 Libraries Guide for HDL Designs](#)

### Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>4/27/07</td>
<td>1.0</td>
<td>Initial Xilinx release.</td>
</tr>
<tr>
<td>4/10/08</td>
<td>1.1</td>
<td>The PLL Module wrapper does not perform any error checking to enforce the design rules and restrictions described in the <em>Virtex-5 User Guide</em>.</td>
</tr>
<tr>
<td>11/17/08</td>
<td>1.2</td>
<td>Incorporated CR473092; corrected PDF properties; converted to current DS template; updated trademark/registration symbol usage; updated links</td>
</tr>
<tr>
<td>6/24/09</td>
<td>1.3</td>
<td>Updated for EDK_L 11.2; created v2.00a.</td>
</tr>
</tbody>
</table>

### Table 2: PLL Module Input and Output Signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKFBIN</td>
<td>Input</td>
<td>Clock feedback input</td>
</tr>
<tr>
<td>CLKin1</td>
<td>Input</td>
<td>Primary clock input</td>
</tr>
<tr>
<td>RST</td>
<td>Input</td>
<td>Asynchronous reset signal</td>
</tr>
</tbody>
</table>
Notice of Disclaimer

Xilinx is providing this design, code, or information (collectively, the “Information”) to you “AS-IS” with no warranty of any kind, express or implied. Xilinx makes no representation that the Information, or any particular implementation thereof, is free from any claims of infringement. You are responsible for obtaining any rights you may require for any implementation based on the Information. All specifications are subject to change without notice. XILINX EXPRESSLY DISCLAIMS ANY WARRANTY WHATSOEVER WITH RESPECT TO THE ADEQUACY OF THE INFORMATION OR ANY IMPLEMENTATION BASED THEREON, INCLUDING BUT NOT LIMITED TO ANY WARRANTIES OR REPRESENTATIONS THAT THIS IMPLEMENTATION IS FREE FROM CLAIMS OF INFRINGEMENT AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Except as stated herein, none of the Information may be copied, reproduced, distributed, republished, downloaded, displayed, posted, or transmitted in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx.