3GPP Searcher v1.0

Introduction

The 3GPP Searcher core is a highly integrated solution for identifying the multiple transmission paths of users in a 3GPP uplink. The core includes all the logic required for scramble code generation, correlation, accumulation, and filtering in a single co-processor, easily integrated with a DSP or microprocessor.

Features

- Device families supported: Virtex™-4, Virtex-5, Spartan™-3A DSP
- Scalable solution for femto-cells to macro-cells
- Algorithm features:
  - Correlation against pilot bit and data bits in DPCCH channel
  - Multiple search correlations in parallel
  - Filtered and unfiltered PDP generation
- High level of integration, encapsulating all circuitry required to generate and maintain PDPs for each search:
  - Automatic scramble code advance
  - Scramble code and pilot generation
  - Search correlation, coherent and non-coherent accumulation
  - PDP filtering
- Design scales with following parameters to minimize resource utilization, based on:
  - Number of searches, results, and antennas
  - Oversample and clock rates
  - Window size
  - Quantization
  - Scheduling period
- Designed for efficient scheduling of searches:
  - Fast changing channels can be scheduled more frequently than slower changing channels, optimizing hardware resources
  - Pipelined firmware operation — new search configurations written concurrently while performing current searches and reading results of previous searches.
  - Design automatically advances scramble code for each search
- Easy integration to microprocessor/DSP via OCP interfaces
  - Pipelined read of search results for speed
  - DMA request interrupt on search configuration interface enables DMA transfers of search configurations

System Overview

Figure 1 shows a typical use of 3GPP Searcher core. The core is designed to act as a co-processor attached to a micro-processor or the DSP processor across a system bus. The open core protocol (OCP) interfaces allow easy adaptation to other bus protocols.

During operation, the processor writes a block of search configurations to the 3GPP Searcher core. This configuration details scrambling code, delay, slot format and associated data. At the start of a search period, the Searcher takes a block of search configurations, and for each search, starts correlating against the incoming antenna data stream. The antenna data stream can come directly from a radio interface, but could also be streamed by DMA across the system bus.

At the end of the search, the resultant power delay profiles (PDPs) for each search can be read across the search results interface on to the system bus.

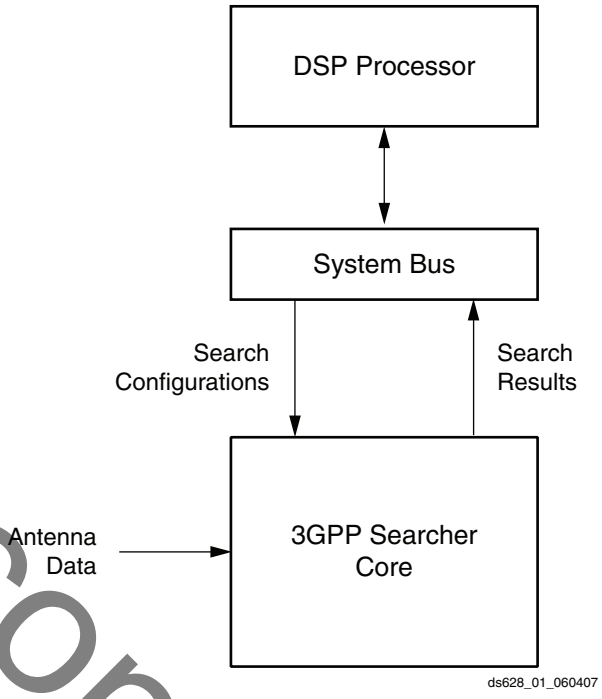

Figure 1: **Typical Application**

Ordering Information

The 3GPP Searcher core is provided under the SignOnce IP Site License and can be generated using the Xilinx CORE Generator system v9.2i or higher. The CORE Generator system is shipped with Xilinx ISE Foundation Series Development software.

Once purchased, the core may be downloaded from the Xilinx IP Center for use with the Xilinx CORE Generator v9.2i and higher. The Xilinx CORE Generator is bundled with the ISE™ Foundation software at no additional charge.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx IP Center .

Revision History

Date	Version	Revision
08/08/07	1.0	Initial Xilinx release