Pinout

Port names for the core module are shown in Figure 1 and described in Table 1. The inclusion of some ports on the module is optional; excluding these ports will alter the function of the module. The optional ports are designated in Table 1.

Clock - CLK

Block Memory is fully synchronous with the clock input. All input pins have setup time referenced to the port CLK pin. The DOUT port has a clock-to-out time referenced to the CLK pin.

By default all memory operations are performed on the rising edge of the clock. Users, however, have the option to perform all memory operations on the rising or the falling edge of the clock. Performing the memory operation on the falling edge of the clock will not use any extra resources.

Enable - EN

The enable pin affects the read, write, and SINIT functionality of the port. When the Block Memory has an inactive enable pin, the output pins are held in the previous state and writing to the memory is disabled.

By default the enable pin is active high. Users, however, have the option to configure the enable pin active high or active low. Configuring the enable pin active low will not use extra resources.

Write Enable - WE

Activating the write enable pin enables writing to the memory locations. When active, the contents of the DIN bus is written to memory at the address pointed to by the ADDR bus. The output latches are loaded or not loaded according to the write configuration (Write First, Read First, No Change). When WE is inactive, a read operation occurs, and the contents of the memory addressed by the ADDR bus are driven on the DOUT bus. In the Read Only port configuration (ROM configuration), the WE pin is not available.

By default the write enable pin is active high. Users, however, have the option to configure the write enable pin active high or active low. Configuring the write enable pin active low will not use extra resources.