

## Introduction

The SPI-3 Physical (PHY) Layer LogiCORE™ IP provides a complete, pre-engineered solution that is fully compatible with the *OIF-SPI3-01.0 System Packet Interface Level-3* implementation agreement. This fully verified solution implements the SPI-3 PHY Layer interface, which interconnects with SPI-3 Link Layer devices.

## Features

- Configurable interface data widths: 8-bit, 16-bit, and 32-bit
- Byte-level and Packet-level transmit flow control configuration options
- Supports 1 to 256 addressable channels
- Fully parameterizable internal FIFO: Depth ranges from 16 to 4096 entries implemented in user-selectable block RAM or distributed memory
- LocalLink user interface allows easy interconnection to other LocalLink-compliant interfaces
- Programmable RX pause value of 0 or 2 cycles
- Greater than 125MHz packet interface supported in Virtex® families; greater than 104MHz packet interface supported in Spartan® families

<b>LogiCORE™ IP Facts</b>					
<b>Core Specifics</b>					
Supported Device Family	Virtex-5, Virtex-4, Spartan-3E, Spartan-3, Spartan-3A/3AN				
Resources Used <sup>1</sup>	I/O	LUTs	FFs	Block RAMs	Slices <sup>2</sup>
Tx Core (8-bit)	24	211	234	1	182
Tx Core (32-bit)	50	222	313	2	230
Rx Core (8-bit)	16	273	272	1	220
Rx Core (32-bit)	42	363	404	2	345
<b>Provided with Core</b>					
Documentation	Product Specification Getting Started Guide				
Design File Formats	VHDL and Verilog				
Constraints File	User Constraints File (UCF)				
Verification	VHDL and Verilog Test Bench				
Instantiation Template	VHDL and Verilog Wrapper				
<b>Design Tool Requirements</b>					
Xilinx Implementation Tools	ISE® v11.1				
Simulation	Mentor Graphics® ModelSim® v6.4b Cadence® IUS v8.1-s009				
Synthesis	XST, Synplify®				
<b>Support</b>					
Provided by Xilinx, Inc. @ <a href="http://www.xilinx.com/support">www.xilinx.com/support</a>					

1. Resources statistics are for a core configured with Packet-level transfer control and a 512-deep block RAM FIFO.
2. Slice counts obtained with area groups placed on each core.















































