LogiCORE IP System Monitor Wizard v2.1

DS608 December 14, 2010 **Product Specification**

Introduction

The LogiCORE™ IP System Monitor Wizard simplifies the instantiation of the System Monitor into the design in Virtex®-5 and Virtex-6 FPGAs. The Wizard creates an HDL file (Verilog or VHDL) that instantiates and configures the System Monitor to customer requirements. See the *Virtex-5 FPGA System Monitor User Guide* [Ref 1] and the *Virtex-6 FPGA System Monitor User Guide* [Ref 2] for detailed descriptions of the System Monitor (SYSMON) functionality.

Features

- Simple user interface
- Easy configuration of various SYSMON modes and parameters
- Simple interface for channel selection and configuration
- Ability to select/deselect alarm outputs
- Ability to set alarm limits
- Calculates all the parameters and register values

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family[1]	Virtex-5[2] LX/LXT/SXT/TXT/FXT Virtex-6[3] LXT/SXT/HXT				
Supported User Interfaces	N/A				
	Resources				**Frequency**
Configuration	**LUTs**	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq.**
Config1	N/A	N/A	N/A	N/A	N/A
Provided with Core					
Documentation	Product Specification Getting Started Guide				
Design Files	Verilog and VHDL				
Example Design	Verilog and VHDL				
Test Bench	Verilog and VHDL				
Constraints File	UCF				
Simulation Model	UNISIM				
Tested Design Tools					
Design Entry Tools	ISE 12.4 [4]				
Simulation	ISim 12.4 Mentor Graphics ModelSim 6.5c Synopsys VCS and VCS MX 2009.12 Cadence IES 9.2				
Synthesis Tools	XST 12.4 Synopsys Synplify Pro 2010.09-1				
Support					
Provided by Xilinx, Inc.					

Notes:

1. For a complete listing of supported devices, see the release notes for this core.
2. For more information on the Virtex-5 devices, see *Virtex-5 Family Overview* [Ref 3]
3. For more information on the Virtex-6 devices, see *Virtex-6 Family Overview* [Ref 4]
4. ISE Service Packs can be downloaded from http://www.xilinx.com/support/download.htm

Functional Description

The System Monitor Wizard is an interactive graphical user interface (GUI) that instantiates a SYSMON based design on specific needs. Using the wizard, users can explicitly configure the SYSMON to operate in the desired mode. The GUI allows the user to select the channels, enable alarms, and set the alarm limits.

SYSMON Functional Features

Major functional SYSMON features can be used to determine an appropriate mode of operation. These features include:

- Analog to digital conversion
- FPGA temperature and voltage monitoring
- Generate alarms based on user set parameters

I/O Signals

Table 1 describes the input and output ports provided from the System Monitor Wizard. Availability of ports is controlled by user-selected parameters. For example, when Dynamic Reconfiguration is selected, these ports are exposed to the user. Any port that is not exposed is appropriately tied off or connected to a signal labeled unused in the delivered source code.

Table 1: **System Monitor I/O Signals**

Port	Direction	Description
DI_IN[15:0]	Input	Input data bus for the dynamic reconfiguration port (DRP).
DO_OUT[15:0]	Output	Output data bus for the dynamic reconfiguration port.
DADDR_IN[6:0]	Input	Address bus for the dynamic reconfiguration port.
DEN_IN	Input	Enable signal for the dynamic reconfiguration port.
DWE_IN	Input	Write enable for the dynamic reconfiguration port.
DCLK_IN	Input	Clock input for the dynamic reconfiguration port.
DRDY_OUT	Output	Data ready signal for the dynamic reconfiguration port.
RESET_IN	Input	Reset signal for the System Monitor control logic and max / min registers.
CONVST_IN	Input	Convert start input. This input is used to control the sampling instant on the ADC input and is only used in Event Mode Timing (see Event-Driven Sampling in the Virtex-5 and Virtex-6 FPGA System Monitor user guides, [Ref 1] and [Ref 2]).
CONVSTCLK_IN	Input	Convert start input. This input is connected to a global clock input on the interconnect. Like CONVST, this input is used to control the sampling instant on the ADC inputs and is only used in Event Mode Timing.
VP_IN VN_IN	Input	One dedicated analog-input pair. The System Monitor has one pair of dedicated analog-input pins that provide a differential analog input.

Table 1: **System Monitor I/O Signals *(Cont'd)***

Port	Direction	Description
VAUXP15[15:0] VAUXN15[15:0]	Inputs	16 auxiliary analog-input pairs. In addition to the dedicated differential analog-input, the System Monitor uses 16 differential digital-input pairs as low-bandwidth differential analog inputs. These inputs are configured as analog during FPGA configuration.
USER_TEMP_ALARM_OUT	Output	System Monitor temperature-sensor alarm output.
VCCINT_ALARM_OUT	Output	System Monitor V_{CCINT}-sensor alarm output.
VCCAUX_ALARM_OUT	Output	System Monitor V_{CCAUX}-sensor alarm output.
OT_OUT	Output	Over-Temperature alarm output.
CHANNEL_OUT[4:0]	Outputs	Channel selection outputs. The ADC input MUX channel selection for the current ADC conversion is placed on these outputs at the end of an ADC conversion.
EOC_OUT	Output	End of Conversion signal. This signal transitions to an active-High at the end of an ADC conversion when the measurement result is written to the status registers. For detailed information, see the System Monitor Timing section in the Virtex-5 and Virtex-6 FPGA System Monitor user guides ([Ref 1] and [Ref 2].)
EOS_OUT	Output	End of Sequence. This signal transitions to an active-High when the measurement data from the last channel in the Channel Sequencer is written to the status registers. For detailed information, see the System Monitor Timing section in the Virtex-5 and Virtex-6 FPGA System Monitor user guides ([Ref 1] and [Ref 2]).
BUSY_OUT	Output	ADC busy signal. This signal transitions High during an ADC conversion. This signal transitions High for an extended period during calibration.
JTAGLOCKED_OUT	Output	Used to indicated that DRP port has been locked by the JTAG interface.
JTAGMODIFIED_OUT	Output	Used to indicate that a JTAG write to the DRP has occurred.
JTAGBUSY_OUT	Output	Used to indicate that a JTAG DRP transaction is in progress.

User Attributes

The System Monitor functionality is configured through the control registers (See the Register File Interface sections in the Virtex-5 and Virtex-6 FPGA System Monitor user guides: [Ref 1] and [Ref 2]). Table 2 lists the attributes associated with these control registers. These control registers can be initialized when the SYSMON primitive is instantiated in the HDL using the attributes listed in Table 2. The control registers can also be initialized through the DRP at run time. The System Monitor Wizard simplifies the initialization of these control registers in the HDL instantiation. The Wizard will generate the correct bit patterns based on user functionality selected through the Wizard GUI.

Table 2: **System Monitor Attributes**

Attribute	Name	Control Reg Address	Description
INIT_40	Configuration register 0	40h	System Monitor configuration registers. For detailed information, see the Virtex-5 and Virtex-6 FPGA System Monitor user guides ([Ref 1] and [Ref 2])
INIT_41	Configuration register 1	41h	
INIT_42	Configuration register 2	42h	
INIT_48 to INIT_4F	Sequence registers	48h to 4Fh	Sequence registers used to program the Channel Sequencer function in the System Monitor. For detailed information, see the Virtex-5 and Virtex-6 FPGA System Monitor user guides ([Ref 1] and [Ref 2]).
INIT_50 to INIT_57	Alarm Limits registers	50h to 57h	Alarm threshold registers for the System Monitor alarm function. For detailed information, see the Virtex-5 and Virtex-6 FPGA System Monitor user guides ([Ref 1] and [Ref 2]).
SIM_MONITOR_FILE	Simulation Analog Entry File	-	This is the text file that contains the analog input stimulus. This is used for simulation.
SIM_DEVICE	Device family	-	This is used to identify the device family. This is used for simulation.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The System Monitor™ Wizard LogiCORE IP core is provided free of charge under the terms of the Xilinx End User License Agreement. The core can be generated by the Xilinx ISE CORE Generator software, which is a standard component of the Xilinx ISE Design Suite. This version of the core can be generated using the ISE CORE Generator system v12.4. For more information, please visit the Architecture Wizards web page.

Information about additional Xilinx LogiCORE modules is available at the Xilinx IP Center. For pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

References

1. UG192, *Virtex-5 FPGA System Monitor User Guide*
2. UG370, *Virtex-6 FPGA System Monitor User Guide*
3. DS100, *Virtex-5 Family Overview*
4. DS150, *Virtex-6 Family Overview*
5. UG741, *System Monitor Wizard Getting Started Guide*

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/15/07	1.0	Initial Xilinx release.
04/19/10	2.0	LogiCORE IP System Monitor Wizard v2.0 release. Updated tools and version numbers. Expanded supported Virtex-5 devices. Added support for Virtex-5 TXT and FXT sub-families. Added Virtex-6 FPGA support. Added Functional Description, SYSMON Functional Features, I/O Signals, Support, Ordering Information, and References.
12/14/10	2.1	Updates to the Wizard and tools versions.

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