

## Introduction

The LogiCORE™ IP Utility Buffer core generates corresponding buffers to bring off-chip signals into internal circuits or out from internal circuits. The core is intended as interconnect logic between off-chip signals and internal circuits.

## Additional Information

See the [product page](#).

## Features

- Configurable size of the signal width
- Configurable buffer type

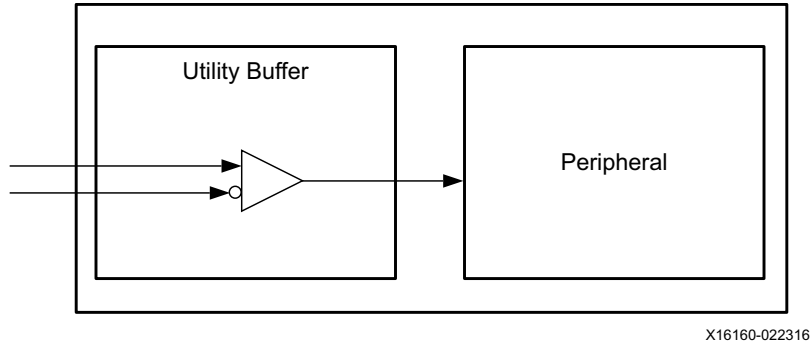
LogiCORE IP Facts Table	
<b>Core Specifics</b>	
Supported Device Family <sup>(1)</sup>	UltraScale+™, UltraScale™ Zynq®-7000 7 Series
Supported User Interfaces	N/A
<b>Provided with Core</b>	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	None
Simulation Model	VHDL
Supported S/W Driver	N/A
<b>Tested Design Flows<sup>(2)</sup></b>	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the <a href="#">Xilinx Design Tools: Release Notes Guide</a> .
Synthesis	N/A
<b>Support</b>	
Provided by Xilinx at the <a href="#">Xilinx Support web page</a>	

### Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).

# Overview

The Utility Buffer core generates corresponding buffers to bring off-chip signals into or out from internal circuits. [Figure 1](#) illustrates the Utility Buffer in a system.

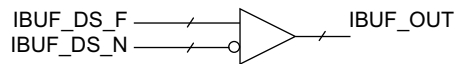


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Figure 1: Utility Buffer in a System

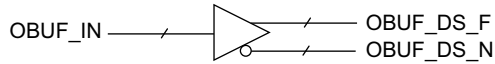
# Block Diagram

**IBUFDS or IBUFGDS**



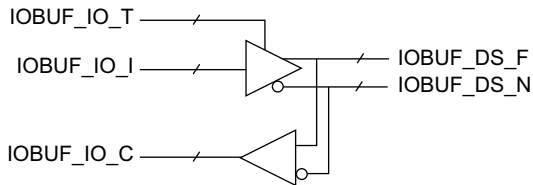
This diagram shows the case where the core instantiates input buffer(s) to bring in off-chip differential signals.

**OBUFDS**



This diagram shows the case where the core instantiates output buffer(s) to bring out internal signals as differential signal pairs.

**IOBUFDS**



This diagram shows the case where the core instantiates three-state buffer(s) for three-state differential signaling I/Os.

X16161-022316

Figure 2: Utility Buffer Block Diagram

# I/O Signals

The Utility Buffer I/O signals are listed and described in [Table 1](#).

**Table 1: Utility Buffer I/O Signals**

Buffer Type	Signal	Interface	I/O	Default Value
IBUFDS	IBUF_DS_P	CLK_IN_D	I	Positive port of the differential input signal.
	IBUF_DS_N	CLK_IN_D	I	Negative port of the differential input signal.
	IBUF_OUT	None	O	Single ended output signal.
OBUFDS	OBUF_IN	None	I	Single ended input signal.
	OBUF_DS_P	None	O	Positive port of the differential output signal.
	OBUF_DS_N	None	O	Negative port of the differential output signal.
IOBUFDS	IOBUF_IO_T	None	I	3-state enable input signal.
	IOBUF_IO_I	None	I	Single ended input signal.
	IOBUF_DS_P	None	O	Positive port of the differential input/output signal.
	IOBUF_DS_N	None	O	Negative port of the differential input/output signal.
	IOBUF_IO_O	None	O	Single ended buffer output signal.
IBUFDSGTE (UltraScale, UltraScale+, and 7 series devices only)	IBUF_DS_P	CLK_IN_D	I	Positive port of the differential input signal.
	IBUF_DS_N	CLK_IN_D	I	Negative port of the differential input signal.
	IBUF_OUT	None	O	Single ended output signal.
	IBUF_DS_ODIV2	None	O	DIV signal that can either output IBUF_OUT or a divide by 2 version of the IBUF_OUT signal.
BUFG	BUFG_I	None	I	Single ended clock input.
	BUFG_O	None	O	Single ended clock output.
BUFGCE	BUFGCE_I	None	I	Single ended clock input of the buffer.
	BUFGCE_CE	None	I	Clock enable input signal of the buffer.
	BUFGCE_O	None	O	Single ended clock output of the buffer.
BUFG GT (UltraScale and UltraScale+ devices only)	BUFG_GT_I	None	I	Buffer input
	BUFG_GT_CE	None	I	Buffer enable
	BUFG_GT_CEMASK	None	I	CE Mask
	BUFG_GT_CLR	None	I	Asynchronous clear forcing the output to zero.
	BUFG_GT_CLRMASK	None	I	CLR Mask.
	BUFG_GT_DIV	None	I	Specifies the value to divide the clock. Divide value is a value provided plus 1. For instance, setting 3'b000 will provide a divide value of 1 and 3'b111 will provide a divide value of 8.
	BUFG_GT_O	None	O	Buffer Output

## Design Parameters

The Utility Buffer design parameters are listed and described in [Table 2](#).

Table 2: Design Parameters

Parameter	Description	Type
C_SIZE	The vector size of differential signal (valid value is 1 to 128)	Integer
C_BUF_TYPE	The buffer to be instantiated (valid values are IBUFDS, OBUFDS, IOBUFDS, IBUFDSGTE, BUFG, BUFGCE, and BUFG GT)	String

## Parameter - Port Dependencies

The parameter and port dependencies are listed and described in [Table 3](#).

Table 3: Parameter and Port Dependencies

Name	Affects	Depends	Relational Description
<b>Design Parameters</b>			
C_Size	All signals	0 to C_SIZE-1	Scale width of all port signals
<b>Port Signals</b>			
IBUF_*	All signals	C_BUF_TYPE	Valid for C_BUF_TYPE=IBUFDS or IBUFGDS, or IBUFDSGTXE, or IBUFDSGTE and not used for other cases
OBUF_*		C_BUF_TYPE	Valid for C_BUF_TYPE=OBUFDS, not used for other cases
IOBUF_*		C_BUF_TYPE	Valid for C_BUF_TYPE=IOBUFDS, not used for other cases

## Design Implementation

### Design Tools

**Note:** This IP can only be used in the Vivado IP integrator. It is not designed to be used in an RTL-only design flow within the Vivado Design Suite.

The Utility Buffer design is handwritten.

### Target Technology

The target technologies are UltraScale+, UltraScale, Zynq-7000, and 7 series devices.

## Device Utilization and Performance Benchmarks

Table 4: Utility Buffer Resource Utilization

Parameter		Resources					
		IBUFDS	IBUFGDS	OBUFDS	IOBUFDS	IBUFDSGTXE	IBUFDSGTE
C_SIZE=n	C_BUF_TYPE=IBUFDS	n	0	0	0	0	0
	C_BUF_TYPE=IBUFGDS	0	n	0	0	0	0
	C_BUF_TYPE=OBUFDS	0	0	n	0	0	0
	C_BUF_TYPE=IOBUFDS	0	0	0	n	0	0
	C_BUF_TYPE=IBUFDSGTXE	0	0	0	0	n	0
	C_BUF_TYPE=IBUFDSGTE	0	0	0	0	0	n

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## Revision History

The following table shows the revision history for this document:

Date	Version	Revision
04/05/2017	2.1	Added 7 series device support for IBUFDSGTE in Table 1 and to the Supported Device Family row in the IP Facts table. Added Automotive Applications disclaimer.
04/06/2016	2.1	Initial Xilinx release of this product brief.

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