LogiCORE IP Spartan-6 FPGA Triple-Rate SDI v1.0

DS849 June 22, 2011 **Product Specification**

Introduction

The LogiCORE™ IP Spartan®-6 FPGA Triple-Rate SDI interface solution provides receiver and transmitter interfaces for the SMPTE SD-SDI, HD-SDI, and 3G-SDI standards. The Spartan-6 FPGA Triple-Rate SDI receiver and transmitter are provided as unencrypted source code in both Verilog and VHDL, allowing the user to fully customize these interfaces as required by specific applications.

Features

- Standards compliance:
  - SMPTE 259 (SD-SDI)
  - SMPTE 292 (HD-SDI)
  - SMPTE 372 (Dual Link HD-SDI)
  - SMPTE 424 and 425 (3G-SDI) including levels A, B-DL, and B-DS
  - SMPTE 352 (Payload ID)
  - SMPTE RP-165 (SD-SDI EDH)
- Triple-Rate SDI receiver features:
  - A single reference clock frequency supports reception of five different bit rates:
    - 270 Mb/s SD-SDI
    - 1.485 Gb/s HD-SDI
    - 1.485/1.001 Gb/s HD-SDI
    - 2.97 Gb/s 3G-SDI
    - 2.97/1.001 Gb/s 3G-SDI
  - Automatically detects incoming SDI standard and bit rate
  - Automatically detects video transport format
  - Detects and captures SMPTE 352 packets
  - Checks for CRC errors for HD-SDI and 3G-SDI
  - Optionally checks for EDH errors for SD-SDI
- Triple-Rate SDI transmitter features:
  - Only two reference clock frequencies are required to transmit five different bit rates:
    - 270 Mb/s SD-SDI
    - 1.485 Gb/s HD-SDI
    - 1.485/1.001 Gb/s HD-SDI
    - 2.97 Gb/s 3G-SDI
    - 2.97/1.001 Gb/s 3G-SDI
  - Generates and inserts CRC and line numbers for HD-SDI and 3G-SDI
  - Generates and inserts EDH packets for SD-SDI
  - Generates and inserts SMPTE 352 packets for all SDI standards

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Spartan-6 Family
Minimum Support Speed Grade	-3
Supported Transceivers	GTP Transceivers
Resources Used	See Table 1
Provided with Core	
Documentation	Product Specification User Guide
Design Files	Verilog and VHDL source code
Example Design	XAPP1076, *Implementing Triple-Rate SDI with Spartan-6 FPGA GTP Transceivers*
Test Bench	Not Provided
Constraints File	User Constraints File (UCF)
Tested Design Tools	
Supported HDL	Verilog and VHDL
Synthesis Tools	XST 13.2
Xilinx Tools	ISE 13.2 software
Simulation Tools(2)	Mentor Graphics ModelSim
Support	
Provided by Xilinx @ www.xilinx.com/support	

1. For a complete listing of supported devices, see the release notes for this core.
2. For the supported versions of the tools, see the *ISE Design Suite 13: Release Notes Guide*.

Applications

- Professional broadcast equipment
- Medical imaging

Resource Utilization

Table 1 lists the resource usage for the LogiCORE IP Spartan-6 FPGA Triple-Rate SDI core.

Table 1: **Resource Usage**

RX only without EDH	
LUTs	2230
Flip-Flops	2010
Slices(1)	1050
BUFG/BUFR	2(2)
PLLADV	1
Block RAMs	2
DSP48A1 Slices	2
Transceivers	1 GTP
RX only with EDH	
LUTs	1660
Flip-Flops	2380
Slices(1)	1300
BUFG/BUFR	2(2)
PLLADV	1
Block RAMs	2
DSP48A1 Slices	2
Transceivers	1 GTP
TX only without EDH	
LUTs	370
Flip-Flops	440
Slices(1)	260
BUFG/BUFR	2(2)
PLLADV	1
Transceivers	1 GTP
TX only with EDH	
LUTs	821
Flip-Flops	810
Slices(1)	520
BUFG/BUFR	2(2)
PLLADV	1
Transceivers	1 GTP

Table 1: **Resource Usage *(Cont'd)***

RX/TX without RX EDH with TX EDH	
LUTs	2880
Flip-Flops	2590
Slices(1)	1440
BUFG/BUFR	4(2)
PLLADV	2
Block RAMs	2
DSP48A1 Slices	2
Transceivers	1 GTP
RX/TX with RX and TX EDH	
LUTs	3300
Flip-Flops	2960
Slices(1)	1700
BUFG/BUFR	4(2)
PLLADV	2
Block RAMs	2
DSP48A1 Slices	2
Transceivers	1 GTP

Notes:

1. Slice counts are only estimates. The exact number of slices depends on level of resource sharing with adjacent logic.
2. Generally, two global or regional clocks are used per RX or TX interface. However, an additional global clock is required to drive the DRPCLK. But, the DRPCLK can be any clock frequency available in the FPGA that falls within the supported DRPCLK frequency range. Multiple SDI interfaces can share the same global DRPCLK.

Supported Video Formats

Table 2 shows the video formats that are supported by the LogiCORE IP Spartan-6 FPGA Triple-Rate SDI core.

Table 2: **Supported Video Formats**

Interface	Video Standard	Sampling Structure / Bit Depth	Frame/Field Rate (Hz)
SD-SDI SMPTE 259-C	PAL	4:2:2 Y'C_B'C_R' 10-bit or 8-bit	50
	NTSC	4:2:2 Y'C_B'C_R' 10-bit or 8-bit	59.94
HD-SDI SMPTE 292	SMPTE 274	4:2:2 Y'C_B'C_R' 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
	SMPTE 296	4:2:2 Y'C_B'C_R' 10-bit	720p: 23.98, 24, 25. 29.97, 30, 50, 59.94, 60
	SMPTE 260	4:2:2 Y'C_B'C_R' 10-bit	1035i: 59.94, 60
	SMPTE 2048-2	4:2:2 Y'C_B'C_R' 10-bit	1080p: 23.98, 24, 25, 29.97, 30

Table 2: **Supported Video Formats *(Cont'd)***

Interface	Video Standard	Sampling Structure / Bit Depth	Frame/Field Rate (Hz)
3G-SDI Level A SMPTE 425-A	SMPTE 274	4:2:2 Y'C_B'C_R' 10-bit	1080p: 50, 59.94, 60
		4:4:4 Y'C_B'C_R' or RGB 10-bit 4:4:4:4 Y'C_B'C_R'A or RGBA 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'C_B'C_R' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'C_B'C_R' 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
	SMPTE 296	4:4:4 or 4:4:4:4 Y'C_B'C_R' or RGB 10-bit	720p: 23.98, 24, 25. 29.97, 30, 50, 59.94, 60
	SMPTE 428-9	4:4:4 X'Y'Z' 12-bit	1080p: 24 1080PsF: 24
	SMPTE 428-19	4:4:4 X'Y'Z' 12-bit	1080p: 25, 30 1080PsF: 25, 30
	SMPTE 2048-2	4:2:2 Y'C_B'C_R' 10-bit	1080p: 47.95, 48, 50, 59.94, 60
		4:4:4 Y'C_B'C_R' or RGB 10-bit 4:4:4:4 Y'C_B'C_R'A or RGBA 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'C_B'C_R' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'C_B'C_R' 12-bit 4:2:2:4 Y'C_B'C_R'A 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
3G-SDI Level B-DL SMPTE 425 B-DL	SMPTE 372	See Dual Link HD-SDI SMPTE 372.	
3G-SDI Level B-DS SMPTE 425 B-DS	2 X HD-SDI streams	See HD-SDI SMPTE 292.	

Table 2: **Supported Video Formats *(Cont'd)***

Interface	Video Standard	Sampling Structure / Bit Depth	Frame/Field Rate (Hz)
Dual Link HD-SDI SMPTE 372	SMPTE 274	4:2:2 Y'C_B'C_R' 10-bit	1080p: 50, 59.94, 60
		4:4:4 or 4:4:4:4 Y'C_B'C_R' or RGB 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'C_B'C_R' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'C_B'C_R' 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
	SMPTE 428-9	4:4:4 X'Y'Z' 12-bit	2048 X 1080p: 24
	SMPTE 428-19	4:4:4 X'Y'Z' 12-bit	1080p: 25, 30 1080PsF: 25, 30
	SMPTE 2048-2	4:2:2 Y'C_B'C_R' 10-bit	1080p: 47.95, 48, 50, 59.94, 60
		4:4:4 Y'C_B'C_R' or RGB 10-bit 4:4:4:4 Y'C_B'C_R'A or RGBA 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'C_B'C_R' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'C_B'C_R' 12-bit 4:2:2 Y'C_B'C_R'A 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30

Functional Overview

The LogiCORE IP Spartan-6 FPGA Triple-Rate SDI solution provides a combined SDI receiver and transmitter core. The SDI receiver and transmitter share a reference clock, but can run at different bit rates and different SDI modes. For example, the receiver can receive a 270 Mb/s SD-SDI signal while the transmitter sends a 2.97/1.001 Gb/s 3G-SDI signal. When both the RX and TX are used, the reference clock frequency is determined by the TX requirements.

The Spartan-6 FPGA Triple-Rate SDI core must be connected to a high-speed transceiver for serialization and deserialization of the SDI bitstream. The core is compatible with the Spartan-6 FPGA GTP transceiver. Figure 1 shows the combined receive/transmit configuration.

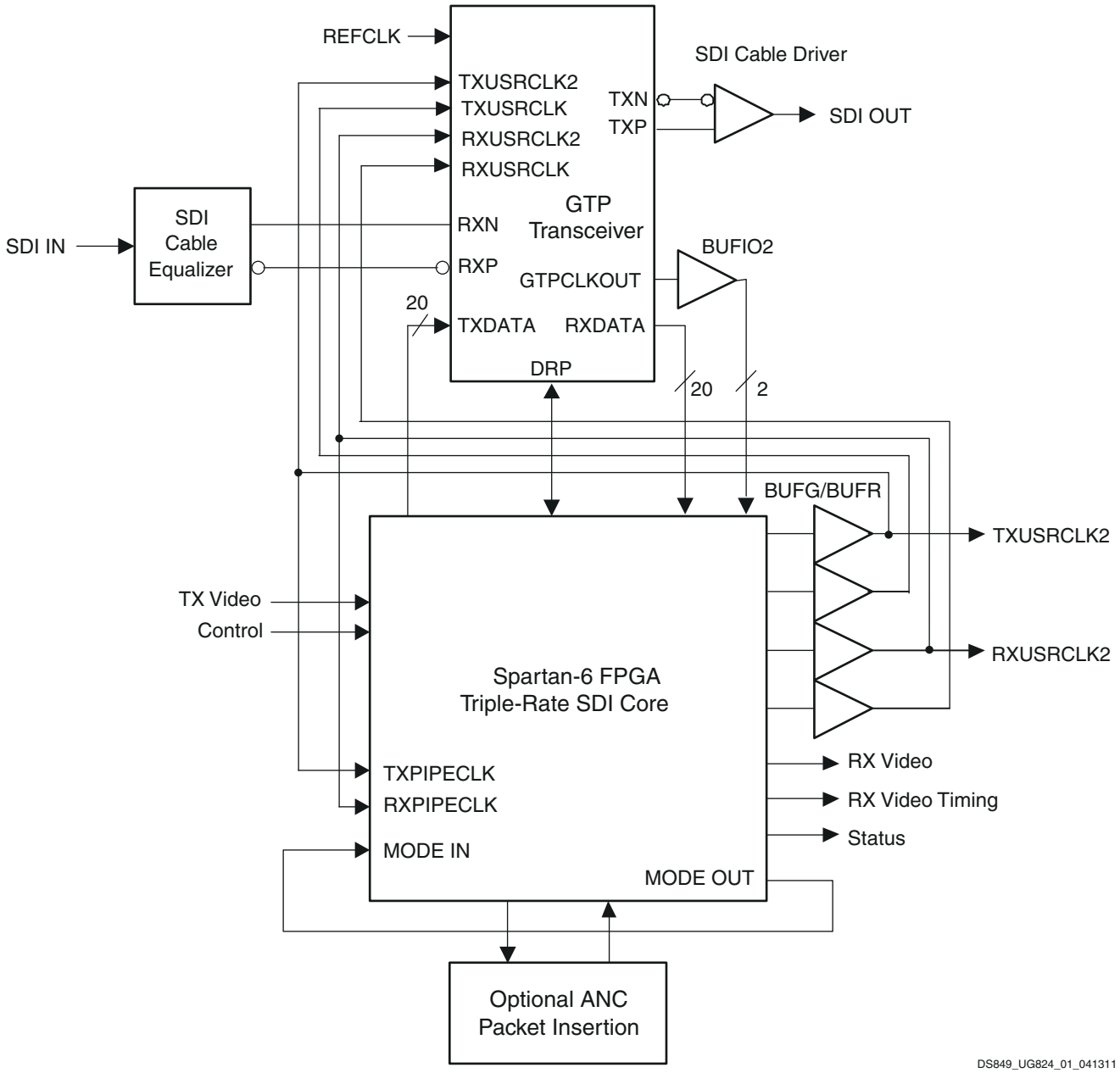

Figure 1: **Triple-Rate SDI RX/TX Functional Overview**

Notes relevant to Figure 1:

1. The required SDI cable driver and cable equalizer are external to the FPGA.
2. The optional ANC packet insertion function is not included in the Spartan-6 FPGA Triple-Rate SDI core.

Combined with a GTP transceiver, the Spartan-6 FPGA Triple-Rate SDI core implements a complete SD-SDI, HD-SDI, and 3G-SDI receiver and/or transmitter interface. The GTP receiver interfaces to the SDI connector through an industry-standard SDI cable equalizer. The GTP transmitter interfaces to the SDI connector through an industry-standard SDI cable driver.

Triple-Rate SDI Receiver Overview

The Triple-Rate SDI receiver uses a single GTP reference clock frequency to receive all five supported SDI bit rates. The receiver automatically determines the incoming SDI bit rate and configures itself and the GTP transceiver appropriately for that SDI mode. The supported GTP receiver reference clock frequencies are: 148.5 MHz and 148.5/1.001 MHz. Either of these frequencies can be used, but only a single frequency is required. The receiver constantly indicates, on dedicated output ports, which SDI mode (SD-SDI, HD-SDI, or 3G-SDI) is currently being received. For HD-SDI and 3G-SDI, it also reports which of the two bit rates supported by these SDI standards is being received. For 3G-SDI, the module also reports whether the data streams are compliant with level A or level B of the SMPTE 425 standard.

The Triple-Rate SDI receiver automatically detects and captures SMPTE 352 payload ID packets in all SDI modes, if they are present. The four user data words captured from these packets are output from the module on dedicated ports.

The Triple-Rate SDI receiver automatically detects transport information about the incoming SDI signal. For SD-SDI, the receiver reports whether the video stream is NTSC or PAL. In HD-SDI and 3G-SDI modes, it reports the SMPTE standards family of the video signal (SMPTE 274, SMPTE 296, etc.), the frame rate, and whether the transport is progressive or interlaced. This information is determined by examining the timing of the SDI transport structure and is, therefore, not dependent on the presence of SMPTE 352 packets. This information represents the transport characteristics, which are not always the same as the picture characteristics. For example, a progressive 1080p 60 Hz picture is carried on an interlaced transport signal in 3G-SDI level B-DL mode. The Triple-Rate SDI receiver accurately reports that the transport is interlaced.

Operation of Triple-Rate SDI Receiver in SD-SDI Mode

In SD-SDI mode, the GTP receiver oversamples the 270 Mb/s SD-SDI bitstream by a factor of 5.5X, and the Triple-Rate SDI receiver uses a digital PLL technique to recover the actual SD-SDI data stream from the oversampled data with a very high level of jitter tolerance. The recovered data is output from the core as a 10-bit interleaved luma/chroma data stream. In SD-SDI mode, the GTP receiver does not recover a clock. Instead, the recovered clock output (GTPCLKOUT[1]) of the GTP receiver is locked to the reference clock. Also the Spartan-6 FPGA Triple-Rate SDI core generates a clock enable that is asserted on any cycle of the rxpipeclk clock in which video data is output from the module, averaging to a 27 MHz output data rate on the 10-bit port. There are, however, several techniques that can be used to produce a true recovered clock in SD-SDI mode. These SD-SDI data recovery techniques are discussed in UG824, *LogiCORE IP Spartan-6 FPGA Triple-Rate SDI User Guide*.

In SD-SDI mode, the Triple-Rate SDI receiver detects SMPTE RP-165 EDH packets. It counts the number of fields that contain EDH packet errors. Also it outputs the received AF, FF, and ANC flags from the EDH packet on dedicated output ports. The EDH function makes the Spartan-6 FPGA Triple-Rate SDI core larger, but it is automatically optimized out of the design if the EDH output ports of the core are not connected.

Operation of the Triple-Rate SDI Receiver in HD-SDI Mode

In HD-SDI mode, the GTP receiver locks to either HD-SDI bit rate (1.485 Gb/s and 1.485/1.001 Gb/s) and recovers the data and a clock. The clock is frequency locked to the incoming HD-SDI bitstream with a nominal frequency of either 74.25 MHz or 74.25/1.001 MHz, depending on the bit rate. The Triple-Rate SDI receiver outputs two 10-bit data streams, one data stream for the luma channel and one for the chroma channel.

The Triple-Rate SDI receiver checks for CRC errors on every video line. It also captures the line number value embedded in the data stream and outputs the captured line number on a dedicated output port.

Operation of the Triple-Rate SDI Receiver in 3G-SDI Mode

In 3G-SDI mode, the GTP receiver locks to either 3G-SDI bit rate (2.97 Gb/s and 2.97/1.001 Gb/s) and recovers the data and a clock. The clock is frequency locked to the incoming 3G-SDI bitstream with a nominal frequency of either 148.5 MHz or 148.5/1.001 MHz, depending on the bit rate. The Triple-Rate SDI receiver automatically detects and reports whether the received data is mapped according to level A or level B of the SMPTE 425 standard.

If the incoming 3G-SDI signal conforms to SMPTE 425 level A, the Triple-Rate SDI receiver outputs two 10-bit data streams fully compatible with SMPTE 425 level A at a nominal rate of 148.5 MHz or 148.5/1.001 MHz. The receiver checks for CRC errors on both data streams. It also captures and outputs the line number from data stream 1. The receiver also captures SMPTE 352 payload ID packets from data stream 1 and outputs the captured user data words on dedicated output ports.

If the incoming 3G-SDI signal conforms to SMPTE 425 level B, the Triple-Rate SDI receiver outputs four 10-bit data streams at a nominal rate of 74.25 MHz or 74.25/1.001 MHz. The receiver checks for CRC errors on all four data streams and captures and outputs the line numbers from the A-Y and B-Y data streams. It also captures and outputs SMPTE 352 packets from both the A data stream pair and the B data stream pair. The user data words from the captured SMPTE 352 packet can be used to determine if the four data streams are compliant with SMPTE 425 level B-DL (dual link) or level B-DS (dual stream). If they are compliant with level B-DL, the data streams carry a single video stream mapped per the SMPTE 372 standard. If they are compliant with level B-DS, data streams carry two separate HD-SDI compatible video streams that were aggregated on a single 3G-SDI signal.

Triple-Rate SDI Transmitter Overview

The Triple-Rate SDI transmitter supports all five supported SDI bit rates, requiring just two different GTP reference clock frequencies to do so. Table 3 shows the supported GTP reference clock frequencies for each bit rate. If 148.5 MHz is used for one reference clock frequency, 148.5/1.001 MHz must be used for the other. Or, if 74.25 MHz is used for one reference clock frequency, 74.25/1.001 MHz must be used for the other. The two reference clock frequencies can be input to the FPGA as one reference clock, using an external switch or a clock generator that can produce either required reference clock frequency or as two separate reference clocks, one of each frequency, using the clock multiplexer built into the GTP transceiver to switch between the two reference clocks.

Table 3: **Triple-Rate SDI TX GTP Reference Clock Frequencies**

SDI Mode	Bit Rate	Required GTP TX REFCLK Frequency
SD-SDI	270 Mb/s	148.5 MHz or 74.25 MHz
HD-SDI	1.485 Gb/s	148.5 MHz or 74.25 MHz
	1.485/1.001 Gb/s	148.5/1.001 MHz or 74.25/1.001 MHz
3G-SDI	2.97 Gb/s	148.5 MHz or 74.25 MHz
	2.97/1.001 Gb/s	148.5/1.001 MHz or 74.25/1.001 MHz

The SDI mode (SD-SDI, HD-SDI, or 3G-SDI) in which the Triple-Rate SDI transmitter is operating is controlled by an input port. Thus, the transmitter can be dynamically switched between SDI modes. In turn, the Triple-Rate SDI transmitter controls the GTP transmitter through the DRP port to configure the GTP transmitter appropriately for each SDI mode.

The Triple-Rate SDI transmitter can generate and insert SMPTE 352 payload ID packets in any SDI mode. The application must supply the four user data words of the SMPTE 352 packet to the transmitter, and the transmitter formats and inserts the packet appropriately.

Operation of the Triple-Rate SDI Transmitter in SD-SDI Mode

In SD-SDI mode, the GTP transmitter is configured to run at a line rate of 2.97 Gb/s. The Triple-Rate SDI transmitter takes in a 10-bit data stream at a 27 MHz rate, optionally calculates and inserts SMPTE RP-168 EDH packets, scrambles the data, and then replicates each bit of the 270 Mb/s bitstream 11 times before sending the data to the GTP transmitter. Because the line rate of the GTP transmitter is 11 times the 270 Mb/s bit rate of the SD-SDI signal and the data provided to the GTP transmitter by the Triple-Rate SDI transmitter has each bit replicated 11 times, the resulting bitstream output by the GTP transmitter is a valid 270 Mb/s SD-SDI bitstream.

The EDH generation and insertion function does make the Triple-Rate SDI transmitter larger. However, if this function is not required, it can be optimized out of the design by permanently disabling EDH insertion.

The 10-bit, 27 MHz data stream supplied to the Triple-Rate SDI transmitter must be an interleaved luma/chroma data stream and must be fully compliant with the SMPTE 259 SD-SDI requirements. Typically, this means that the input data streams should have EAV and SAV sequences at the appropriate places. But, for SD-SDI mode only, the transmitter has a video flywheel that generates and inserts EAV and SAV sequences if they are missing. This flywheel only works in SD-SDI mode and only if insertion of EDH packets is enabled.

Operation of the Triple-Rate SDI Transmitter in HD-SDI Mode

In HD-SDI mode, the Triple-Rate SDI transmitter takes in two 10-bit data streams, one data stream for the luma channel and one for the chroma channel. These data streams must be fully compliant with SMPTE 274, SMPTE 296, or SMPTE 2048-2, as specified by the SMPTE 292 HD-SDI standard. Thus the data stream must have EAV and SAV sequences at the appropriate places. The Triple-Rate SDI transmitter optionally inserts line numbers and calculates and inserts CRC values into the data streams in the appropriate words immediately after the EAV sequence. The data streams are interleaved and scrambled, and then output to the GTP transmitter for serialization.

As previously described, the Triple-Rate SDI transmitter can optionally generate and insert SMPTE 352 payload ID packets. In the case of HD-SDI, these packets are inserted in the luma channel only on specific lines that are dependent upon the video format. The SMPTE 352 standard requires that these packets be placed at the beginning of the HANC space, immediately after the CRC words that follow the EAV. Following the SMPTE 352 packet, applications might need to insert other ancillary data packets, such as embedded audio packets. It is best to allow the Triple-Rate SDI transmitter to insert the SMPTE 352 packets first, before the application begins inserting other packets in the HANC space, to ensure that the SMPTE 352 packets do, in fact, appear at the beginning of the HANC space. To facilitate this, the Triple-Rate SDI transmitter provides datapaths to output the data streams after they have passed through the SMPTE 352 insertion function. These data streams can then be processed by other application-specific modules to insert other ancillary data packets, before going back into the Triple-Rate SDI transmitter on another set of data stream input ports for final processing. The output data streams from the Triple-Rate SDI transmitter after SMPTE 352 packet insertion do not yet have line numbers and CRC words inserted by the transmitter.

Operation of the Triple-Rate SDI Transmitter in 3G-SDI Mode

In 3G-SDI mode, the Triple-Rate SDI transmitter accepts either two or four 10-bit data streams depending on the SMPTE 425 level.

For level A, two input data streams are accepted at a nominal rate of 148.5 MHz or 148.5/1.001 MHz. These data streams must be fully compliant with SMPTE 274, SMPTE 296, SMPTE 2048-2, SMPTE 428-9, or SMPTE 428-19 as specified by the SMPTE 425 standard. The transmitter optionally inserts SMPTE 352 packets into both data streams and outputs the data streams for further ancillary data packet insertion, as described in the HD-SDI section. The transmitter optionally inserts line number words and generates and inserts CRC words into both data streams. The data streams are interleaved and scrambled and then output to the GTP transmitter for serialization.

For level B, four input data streams are accepted at a nominal rate of 74.25 MHz or 74.25/1.001 MHz. For level B-DL, these four data streams must conform to the SMPTE 372 standard. For level B-DS, these four data streams are two luma and chroma data stream pairs, one pair for each of two separate HD-SDI signals to be aggregated and transported on the 3G-SDI interface.

For level B, the transmitter optionally inserts SMPTE 352 packets into the A-Y and B-Y data streams and then outputs all four data streams for further ancillary data packet insertion. The transmitter optionally inserts line number words and generates and inserts CRC words into all four data streams. The data streams are interleaved and scrambled and then output to the GTP transmitter for serialization.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

This Xilinx® LogiCORE IP module is provided under the terms of the Xilinx End User License Agreement. The core is generated using the CORE Generator™ software provided with the Xilinx ISE® Design Suite.

Contact your local Xilinx sales representative for information on pricing and availability of other Xilinx LogiCORE IP modules. Information about additional modules can be found at the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/22/11	1.0	Initial Xilinx release.

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