Xilinx MicroBlaze™ Trace Core (XMTC) (v1.00c)

DS642 April 24, 2009 **Product Specification**

Introduction

This document provides the design specification for the Xilinx MicroBlaze™ Trace Core (XMTC), which provides instruction and data trace capabilities for MicroBlaze processors.

Features

- MicroBlaze instruction and data trace encoding
- Support for MicroBlaze trace interface version 1 (MBTRACE) in MicroBlaze processor version 6
- Support for MicroBlaze trace interface version 2 (MBTRACE2) in MicroBlaze processor version 7
- Communicates with debugger using JTAG protocol through the MicroBLaze Debug Module (MDM)
- Configurable output trace clock for Support for Single Data Rate (SDR) or Dual Data Rate (DDR)
- Support for configurable number of trigger conditions

LogiCORE™ IP Facts				
Core Specifics				
Supported Device Family(1)	See EDK Supported Device Families.			
Version of Core	xmtc		v1.00c	
Resources Used	I/O	LUTs	FFs	Block RAMs
	Not Available			
Provided with Core				
Documentation	Product Specification			
Design File Formats	VHDL			
Design Tool Requirements				
Xilinx Implementation Tools	See Tools for requirements.			
Verification				
Simulation				
Synthesis				
Support				
Provided by Xilinx, Inc.				

1. Example of a table footnote.

Functional Description

XMTC enables tracing capabilities on MicroBlaze processors. It contains an input interface that attaches to a MicroBlaze Trace port composed of approximately 200 un-encoded signals and an output interface that provides an encoded trace in 22 signals. The block diagram of the core is shown in Figure 1.

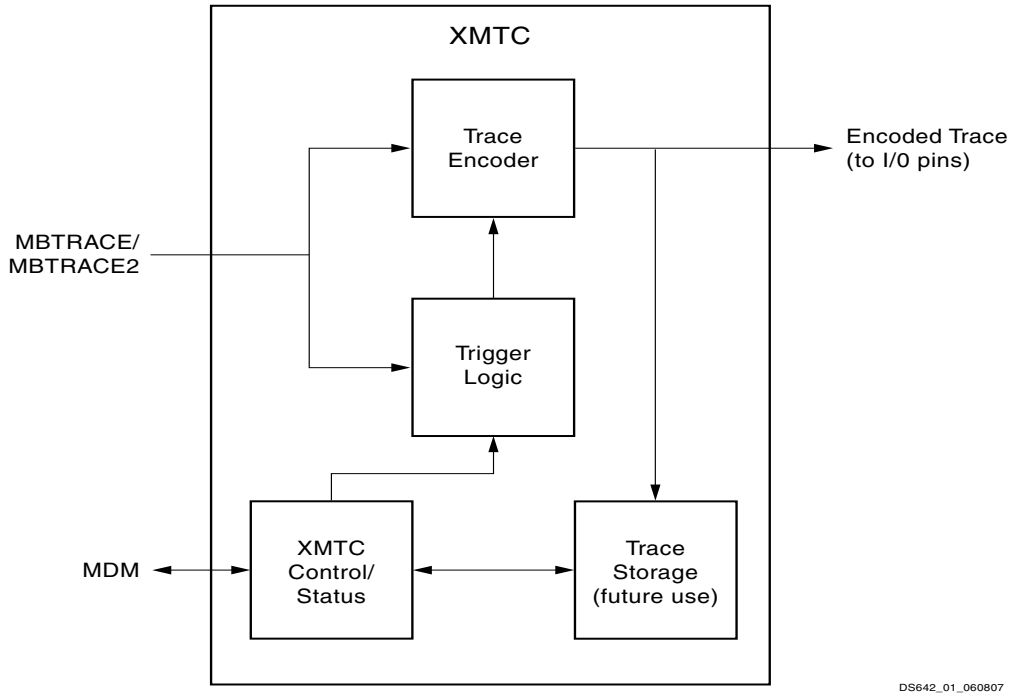

Figure 1: **XMTC Block Diagram**

XMTC supports the two MicroBlaze Trace interface versions. The input trace port can be configured for MicroBlaze trace version 1 (MBTRACE), available in MicroBlaze version 6; or it can be configured for MicroBlaze trace version 2 (MBTRACE2), available MicroBlaze version 7. The core cannot use both interfaces at the same time.

XMTC I/O Signals

The I/O signals in XMTC are listed and described in Table 1.

Table 1: **XMTC I/O Signals**

Signal Name	Interface	I/O	Initial State	Description
Clk		I		Clock
Rst		I		Reset
MicroBlaze Trace Signals				
Trace_Instr_Valid	MBTRACE / MBTRACE2	I		Valid instruction on trace port
Trace_Instruction[0:31]	MBTRACE / MBTRACE2	I		Instruction code

Table 1: **XMTC I/O Signals *(Cont'd)***

Signal Name	Interface	I/O	Initial State	Description
Trace_PC[0:31]	MBTRACE / MBTRACE2	I		Program counter
Trace_Reg_Write	MBTRACE / MBTRACE2	I		Instruction writes to the register file
Trace_Reg_Addr[0:4]	MBTRACE / MBTRACE2	I		Destination register address
Trace_MSR_Reg_11[0:10]	MBTRACE	I		Machine status register
Trace_MSR_Reg_15[0:14]	MBTRACE2	I		
Trace_PID_Reg	MBTRACE2	I		Process identifier register
Trace_New_Reg_Value[0:31]	MBTRACE / MBTRACE2	I		Destination register update value
Trace_Exception_Taken	MBTRACE / MBTRACE2	I		Instruction result in taken exception
Trace_Exception_Kind_4[0:3]	MBTRACE	I		Exception type
Trace_Exception_Kind_5[0:4]	MBTRACE2	I		
Trace_Jump_Taken	MBTRACE / MBTRACE2	I		Branch instruction evaluated true and is taken
Trace_Delay_Slot	MBTRACE / MBTRACE2	I		Instruction is in delay slot of a taken branch
Trace_Data_Access	MBTRACE / MBTRACE2	I		Valid D-side memory access
Trace_Data_Adress[0:31]	MBTRACE / MBTRACE2	I		Address for D-side memory access
Trace_Data_Write_Value[0:31]	MBTRACE / MBTRACE2	I		Value for D-side memory access
Trace_Data_Byte_Enable[0:3]	MBTRACE / MBTRACE2	I		Byte enables for D-side memory access
Trace_Data_Read	MBTRACE / MBTRACE2	I		D-side memory access is a read
Trace_Data_Write	MBTRACE / MBTRACE2	I		D-side memory access is a write
Trace_DCache_Req	MBTRACE / MBTRACE2	I		Data memory address is within D-cache range
Trace_DCache_Hit	MBTRACE / MBTRACE2	I		Data memory address is present in D-Cache
Trace_ICache_Req	MBTRACE / MBTRACE2	I		Instruction memory address is in I-Cache range
Trace_ICache_Hit	MBTRACE / MBTRACE2	I		Instruction memory address is present in I-Cache
Trace_OF_Piperun	MBTRACE / MBTRACE2	I		Pipeline advance for Decode stage
Trace_EX_Piperun	MBTRACE / MBTRACE2	I		Pipeline advance for Execution stage

Table 1: **XMTC I/O Signals *(Cont'd)***

Signal Name	Interface	I/O	Initial State	Description
Trace_MEM_Piperun	MBTRACE / MBTRACE2	I		Pipeline advance for Memory stage
Debug Signals				
Trace_MB_Halted		I		MicroBlaze is in Debug Mode
MDM Interface Signals				
MDM_TDI	MDM	I		BSCAN test data in
MDM_SEL	MDM	I		BSCAN select
MDM_SHIFT	MDM	I		BSCAN shift
MDM_UPDATE	MDM	I		BSCAN update
MDM_RESET	MDM	I		BSCAN reset
MDM_DRCK	MDM	I		BSCAN clock
MDM_CAPTURE	MDM	I		BSCAN capture
MDM_TDO	MDM	O		BSCAN test data out
MicroBlaze Trace Core Signals				
XMTC_Clk	XMTC	O		Encoded trace output clock
XMTC_Data[0:17]	XMTC	O		Encoded trace data
XMTC_Collect	XMTC	O		Trace collect
XMTC_Trig_Out	XMTC	O		Trace trigger output
XMTC_Trig_In	XMTC	I		Trace trigger input

XMTC Design Parameters

Table 2 lists and describes the features that can be parameterized in the Xilinx MicroBlaze Trace Core.

Table 2: **MDM Design Parameters**

Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
System Parameters				
Target FPGA family	C_FAMILY	spartan3, spartan3e, spartan3a, spartan3an, virtex4, virtex5	virtex5	string
Instance name	C_INSTANCE	valid string	xmtc_inst	string
Trace Parameters				
MicroBlaze Trace Version(1)	C_TRACE_VERSION	1 = MBTRACE 2 = MBTRACE2	2	integer
Output Clock Style	C_CLOCK_STYLE	1 = SDR 2 = DDR	2	integer
External input reset high	C_EXT_RESET_HIGH	0,1	1	integer

Table 2: **MDM Design Parameters**

Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Trigger Parameters				
Command count	C_COMMAND_COUNT	1-16	1	integer
PC comparator count	C_PC_COMPARATOR _COUNT	0-2	0	integer
Read address comparator count	C_RA_COMPARATOR _COUNT	0-2	0	integer
Write address comparator count	C_WA_COMPARATOR _COUNT	0-2	0	integer
Counter count	C_COUNTER_COUNT	0-2	0	integer
Data value comparator count	C_DATAVAL_COUNT	0-2	0	integer
Register value comparator count	C_REGVAL_COUNT	0-2	0	integer
Encoder Parameters				
Always Collect	C_ALWAYS_COLLECT	0,1	1	integer
Storage Parameters				
Enable on-chip storage (future)(2)	C_ONCHIP_STORAGE	0,1	0	integer
On-chip storage size (future)(2)	C_STORAGE _KSAMPLES	1-16	1	integer

1. MicroBlaze Trace Version 1 (MBTRACE) is used in MicroBlaze v6. MicroBlaze Trace version 2 (MBTRACE2) is used in MicroBlaze v7.
2. Not implemented in this version.

Allowable Parameter Combinations

There are currently no restrictions on parameter combinations for this core.

Parameter-Port Dependencies

The MBTRACE interface is only available when C_TRACE_VERSION = 1. The MBTRACE2 interface is only available when C_TRACE_VERSION = 2.

XMTC Registers

The registers in XMTC are accessible only through JTAG and are only to be accessed by Xilinx or third-party debug and trace tools.

XMTC Interrupts

The XMTC does not generate interrupts.

Design Implementation

Target Technology

For targeted FPGA families, see EDK Supported Device Families.

Device Utilization and Performance Benchmarks

Not available.

Specification Exceptions

None.

Reference Documents

The XMTC core is to be used with third-party software. For more information on how to trace using XMTC, consult the third-party software documentation.

For connector and pin-out information, please consult the third party hardware documentation.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Revision History

Date	Version	Revision
6/26/2007	1.0	Initial Xilinx release.
11/20/2007	1.1	Updated trace port width, Table 1 title and Reference Documents.
4/28/2008	1.2	Added Automotive Spartan®-3E, Automotive Spartan-3A, Automotive Spartan-3 and Automotive Spartan-3A DSP; added Spartan-3A DSP.
6/25/2008	1.3	Added QPro Virtex®-4 Hi-Rel and QPro Virtex-4 Rad Tolerant.
4/24/2009	1.4	Replaced references to supported device families and tool names with hyperlink to PDF file.

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