

## Introduction

The XPS Thin Film Transistor (TFT) controller is a hardware display controller IP core capable of displaying 256k colors. The XPS TFT controller connects as a master on the PLB V4.6 (Processor Local Bus with Xilinx simplification) and reads the video pixel data from PLB attached video memory. This core also connects as a slave to the PLB or DCR (Device Control Register) bus for the register access. This core is capable of configuring Chrontel CH-7301 DVI Transmitter Chip through I2C interface.

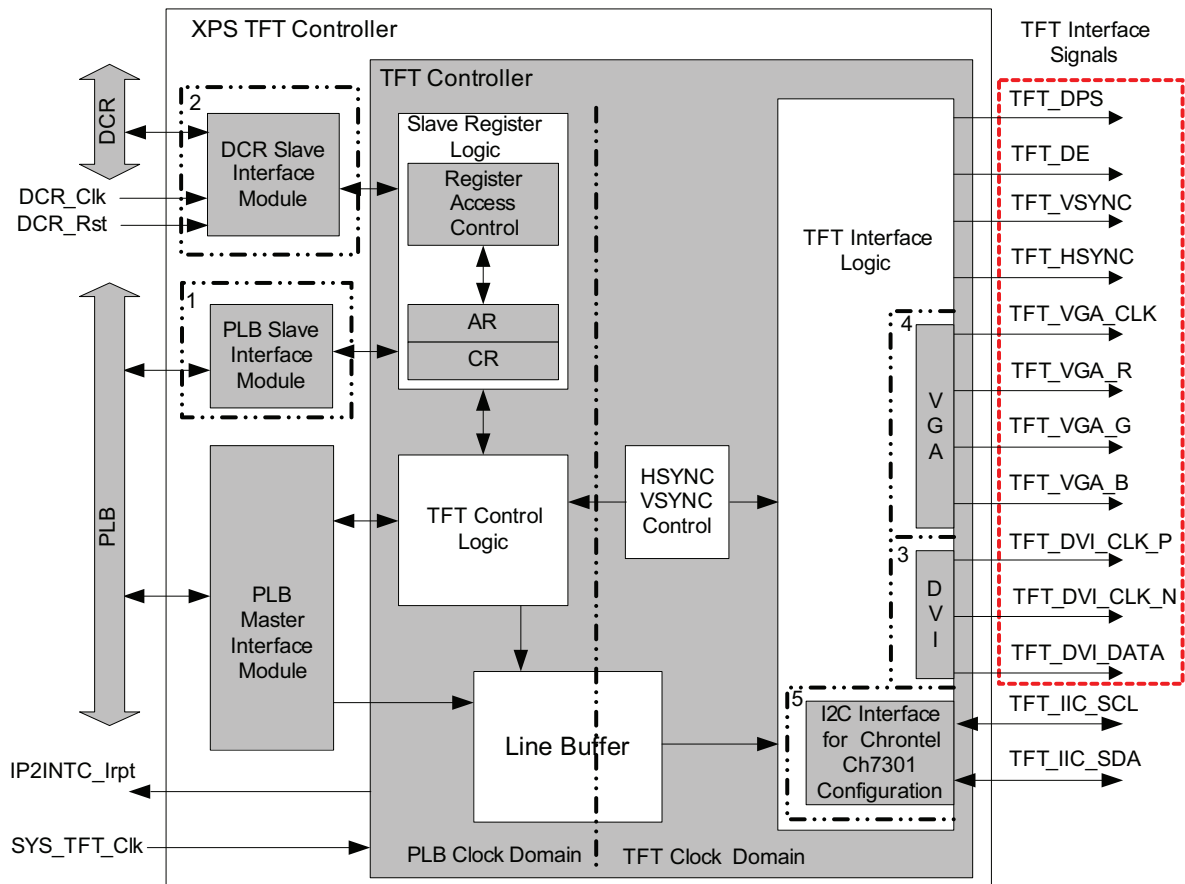
## Features

- Connects as 64-bit master on PLB V4.6 bus of 64 or 128 bits data width
- Connects as a 32-bit Slave on the DCR V2.9 bus or PLB V4.6 bus of 32, 64 and 128 bits data width
- Supports DCR daisy chain protocol
- Parameterizable TFT interface for 18-bit VGA or 24-bit DVI
- Supports 25 Mhz TFT clock for display resolution of 640x480 pixels at 60 Hz refresh rate
- Supports configuration of external Chrontel DVI Transmitter Chip through I2C interface
- Supports separate clock domain for PLB interface and TFT interface
- Supports Vsync Interrupt and Status

| LogiCORE™ Facts                          |  |        |
|--|--|--------|
| Core Specifics                           |  |        |
| Supported Device Family                  | Virtex-4®, Virtex-4Q, Virtex-4QV, Virtex-5, Virtex-5FX, Virtex-6, Virtex-6CX, Spartan®-3E, Automotive Spartan-3E, Spartan-3, Automotive Spartan-3, Spartan-3A, Automotive Spartan-3A, Spartan-3A DSP, Automotive Spartan-3A DSP, Spartan-6 |        |
| Version of core                          | xps_tft  | v2.00a |
| Resources Used                           |  |        |
|  | Min  | Max    |
| SLICES                                   | Refer to the <a href="#">Table 13</a> , <a href="#">Table 14</a> , <a href="#">Table 15</a> and <a href="#">Table 16</a>   |        |
| LUTs                                     |  |        |
| FFs                                      |  |        |
| Block RAMs                               | 1  |        |
| Special Features                         | N/A  |        |
| Provided with Core                       |  |        |
| Documentation                            | Product Specification  |        |
| Design File Formats                      | Mixed  |        |
| Constraints File                         | N/A  |        |
| Verification                             | N/A  |        |
| Instantiation Template                   | N/A  |        |
| Design Tool Requirements                 |  |        |
| Xilinx Implementation Tools              | ISE® 11.3 or later   |        |
| Verification                             | Mentor Graphics ModelSim v6.4b or later  |        |
| Simulation                               | Mentor Graphics ModelSim v6.4b or later  |        |
| Synthesis                                | XST 11.3or later   |        |
| Support                                  |  |        |
| Provided by <a href="#">Xilinx, Inc.</a> |  |        |

## Functional Description

The XPS TFT controller is a hardware display controller for a 640x480 resolution display screen. This core is capable of displaying up to 256K colors through VGA or DVI interface. The design contains PLB master interface that reads video data from a PLB attached memory device and displays the data onto the TFT screen. The design also contains parameterizable DCR and PLB slave interface. If the parameter C\_DCR\_SPLB\_SLAVE\_IF is set to 1, the controller can be configured using PLB slave interface, else it can be configured through DCR slave interface. This controller also provide I2C interface to configure Chrontel CH7301C video encoder chip when the DVI interface is selected. The XPS TFT controller block diagram is shown in [Figure 1](#).



Note:

1. PLB Slave Interface is included in the design if the parameter C\_DCR\_SPLB\_SLAVE\_IF = 1.
2. DCR slave interface is part of Slave Register Logic and included in the design if the parameter C\_DCR\_SPLB\_SLAVE\_IF = 0.
3. DVI interface is included in the design if the parameter C\_TFT\_INTERFACE = 1.
4. VGA interface is included in the design if the parameter C\_TFT\_INTERFACE = 0.
5. This logic is included in the design if C\_TFT\_INTERFACE = 1.

DS695\_01\_020509

Figure 1: XPS TFT Controller Block Diagram

The major modules of XPS TFT controller are described in subsequent sections.

These modules are:

- PLB Master Interface Module
- PLB Slave Interface Module
- Slave Register Logic
- TFT Control Logic
- Line Buffer
- HSYNC VSYNC Control
- TFT Interface Logic

### **PLB Master Interface Module**

The PLB Master Interface Module provides master interface between TFT controller and the PLB. TFT controller reads pixel data from an external PLB memory device through PLB Master Interface Module. This module takes care of bus interface signals, bus protocol and other interface issues. The master interface native data width is fixed to 64-bits. The C\_MPLB\_SMALLEST\_SLAVE size should be same as the PLB attached memory data width.

### **PLB Slave Interface Module**

The PLB Slave Interface Module provides interface between Slave Register Logic and PLB bus. This interface is included in the design if parameter C\_DCR\_SPLB\_SLAVE\_IF is set to 1. The XPS TFT controller registers can be accessed through PLB using this interface. The XPS TFT controller core only supports 1:1 and 1:2 clock ratio for SPLB to MPLB clocks.

### **Slave Register Logic**

The Slave Register Logic module consists of Address Register (AR), Control Register (CR) and logic to provide the access to these registers using either PLB or DCR interface. The DCR slave interface logic is included in the design if the parameter C\_DCR\_SPLB\_SLAVE\_IF is set to 0. The Address Register allows user to change the base address of video memory to be read from. This allows video frames to be fetched from other memory locations without being seen on the display. The user can change the video memory base address to display a different frame when it is ready. The Control Register allows the display to be rotated by 180 degrees or turned off by configuring the control bits.

### **TFT Control Logic**

The TFT Control Logic module generates read request to PLB Master Interface Module to get pixel data from an external PLB memory device. This module synchronizes the signals crossing the different clock domains. The TFT control logic generates master read request, address for the video memory and reads the pixel data for each display line using a series of 16-double word burst transactions. The pixel data is stored in an internal line buffer and then sent out to TFT display with the necessary timing to correctly display the image. This process repeats continuously over every line and frame to be displayed on the 640x480 TFT screen. The data flow diagram from PLB to TFT is shown in **Figure 2**. When the display is turned off by clearing the display enable bit in the Control Register, the TFT controller issues reset to all the counters and stops requesting data from the video memory by applying reset to the Master Interface Module. In the reset state, the controller sets the Hsync and Vsync to their default value causing the display to enter in sleep mode.

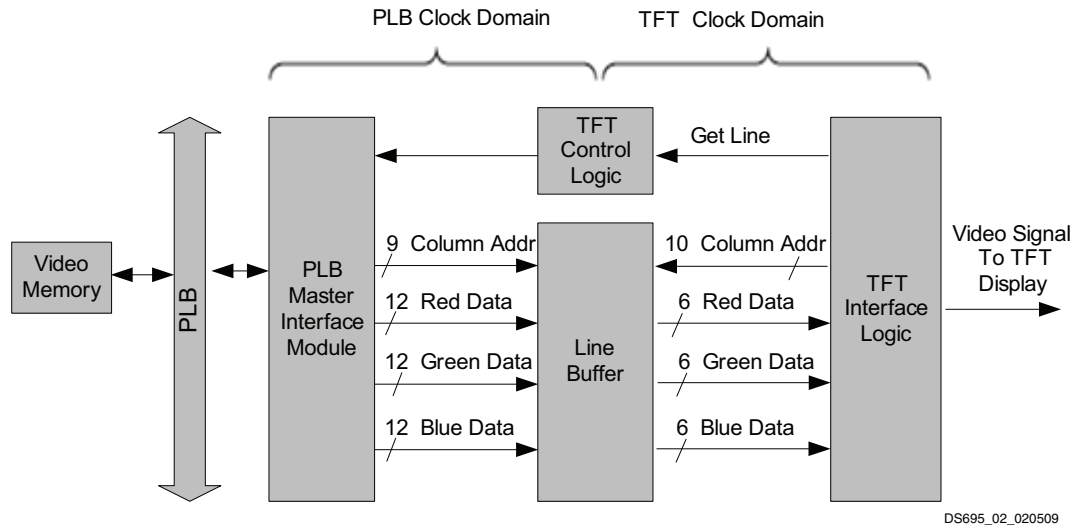


Figure 2: Data Flow Diagram

### Line Buffer

The XPS TFT controller allows PLB clock and TFT video clock to be asynchronous to each other. The line buffer module includes synchronization logic to allow control signals to be passed between asynchronous PLB and TFT clock domains. This module consists of a dual port BRAM of size 1KB x 18 bit which is used as the line buffer to pass video data between the two clock domains. Out of 64-bit PLB data, the 36-bit of RGB data gets written to the BRAM.

### HSYNC/VSYNC Control

This module generates the necessary timing of all the video synchronization signals including back porch and front porch timing for Hsync and Vsync. See [Video Timing](#) section for more information.

### TFT Interface Logic

The TFT interface logic driving the TFT display operates in the same clock domain as the video clock. It reads out the pixel data from the dual port line buffer and transmits it to the TFT. This module consists of logic to transmit the pixel data in either VGA or DVI format based on the parameter C\_TFT\_INTERFACE and the logic to configure the Chrontel CH-7301 video encoder chip. The Hsync, Vsync and DE signals are common for both the interfaces. The VGA, DVI and Chrontel I2C interfaces are described below.

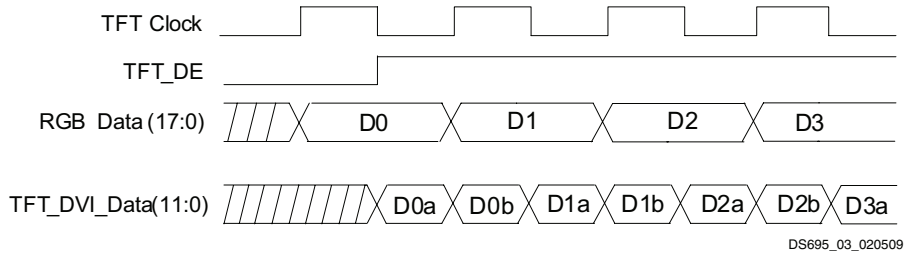
### VGA Interface

The VGA interface logic is included in the design if the parameter C\_TFT\_INTERFACE is set to 0. The 18-bit RGB pixel data is transmitted to the VGA ports and logic '0' is transmitted to all DVI ports.

### DVI Interface

The DVI interface logic is included in the design if the parameter C\_TFT\_INTERFACE is set to 1. The 18-bit RGB data is converted into 24-bit pixel data by padding zeros in between the RGB data. This 24-bit pixel data is transmitted to the 12-bit DVI data port by clocking the data on both edges using

double data rate registers as shown in **Figure 3**. The 18-bit RGB pixel data translation to 24-bit DVI data is shown in **Table 1**.



DS695\_03\_020509

Figure 3: RGB to DVI data

Table 1: RGB to DVI data conversion

| DVI Data         | Data A | Data B |
|------------------|--------|--------|
| TFT_DVI_DATA[0]  | G[2]   | 0      |
| TFT_DVI_DATA[1]  | G[3]   | 0      |
| TFT_DVI_DATA[2]  | G[4]   | B[0]   |
| TFT_DVI_DATA[3]  | G[5]   | B[1]   |
| TFT_DVI_DATA[4]  | 0      | B[2]   |
| TFT_DVI_DATA[5]  | 0      | B[3]   |
| TFT_DVI_DATA[6]  | R[0]   | B[4]   |
| TFT_DVI_DATA[7]  | R[1]   | B[5]   |
| TFT_DVI_DATA[8]  | R[2]   | 0      |
| TFT_DVI_DATA[9]  | R[3]   | 0      |
| TFT_DVI_DATA[10] | R[4]   | G[0]   |
| TFT_DVI_DATA[11] | R[5]   | G[1]   |

### Chrontel I2C Interface

The Chrontel I2C interface logic is included in the design if the parameter C\_TFT\_INTERFACE is set to 1. This module consists of logic to configure the Chrontel CH-7301 video encoder chip. The configuration sequence logic is hard coded in this module and the data is sent over I2C interface. This core configures only the basic registers of the CH-7301 chip for DVI interface. The XPS TFT controller remains in the reset state till the controller completes configuration of the Chrontel chip. The description of these registers address and the configuration data is shown in Table 2. If the user wants different configuration for the Chrontel chip, then user must configure the Chrontel chip externally. For more information on the Chrontel DVI transmitter, please refer the Chrontel CH7301 DVI Transmitter Device Specification.

Table 2: Chrontel CH-7301 Configuration Register Description

| Register Address (hex) | Register Name | Configuration Data (hex) | Access | Description                      |
|------------------------|---------------|--------------------------|--------|----------------------------------|
| 49                     | PM            | C0                       | Write  | Power Management Register        |
| 21                     | DC            | 09                       | Write  | DAC Control Register             |
| 33                     | TPCP          | 08                       | Write  | PLL Charge Pump Control Register |
| 34                     | TPD           | 16                       | Write  | PLL Divider Register             |
| 36                     | TPF           | 60                       | Write  | PLL Filter Register              |

### Video Timing

The signal timings for 640x480 display using a 25 MHz pixel clock are shown in Table 3. The XPS TFT controller takes 16.8 ms to display each 640x480 display frame at 60 Hz refresh rate on the TFT. Hence, to display the complete frame on the TFT, user should not update the video memory start address (AR) before this time frame.

Table 3: 640x480 Mode Display Timing

| Symbol             | Parameter        | Vertical Sync |        |       | Horizontal Sync |        |
|--------------------|------------------|---------------|--------|-------|-----------------|--------|
|                    |                  | Time          | Clocks | Lines | Time            | Clocks |
| T <sub>PULSE</sub> | Sync pulse time  | 16.8 ms       | 420000 | 525   | 32 $\mu$ s      | 800    |
| T <sub>Disp</sub>  | Display time     | 15.4 ms       | 384000 | 480   | 25.6 $\mu$ s    | 640    |
| T <sub>PW</sub>    | Pulse width time | 64 $\mu$ s    | 1600   | 2     | 3.84 $\mu$ s    | 96     |
| T <sub>BP</sub>    | Back porch time  | 992 $\mu$ s   | 24800  | 31    | 1.92 $\mu$ s    | 48     |
| T <sub>FP</sub>    | Front porch time | 384 $\mu$ s   | 9600   | 12    | 640 ns          | 16     |

### Hsync Timing

The Hsync is active low signal and the complete time period of the Hsync is 800 TFT clocks. Out of the 800 TFT clock period, the active pixel data qualified by the active high DE signal is of 640 TFT clocks. The Hsync pulse period is of 96 TFT clocks. The time period between the Hsync pulse and start of active data is called as back porch which is of 48 TFT clocks. The time period between the end of active data and start of new Hsync pulse is called as front porch which is of 16 TFT clocks. The Hsync timing with respect to the TFT clock is shown in [Figure 4](#).

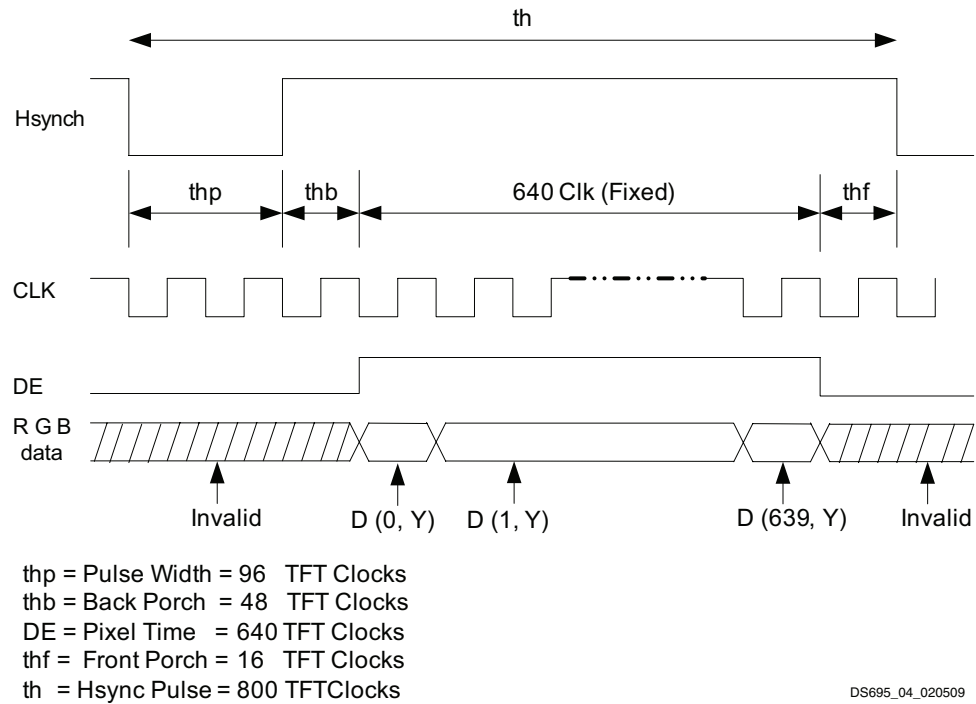
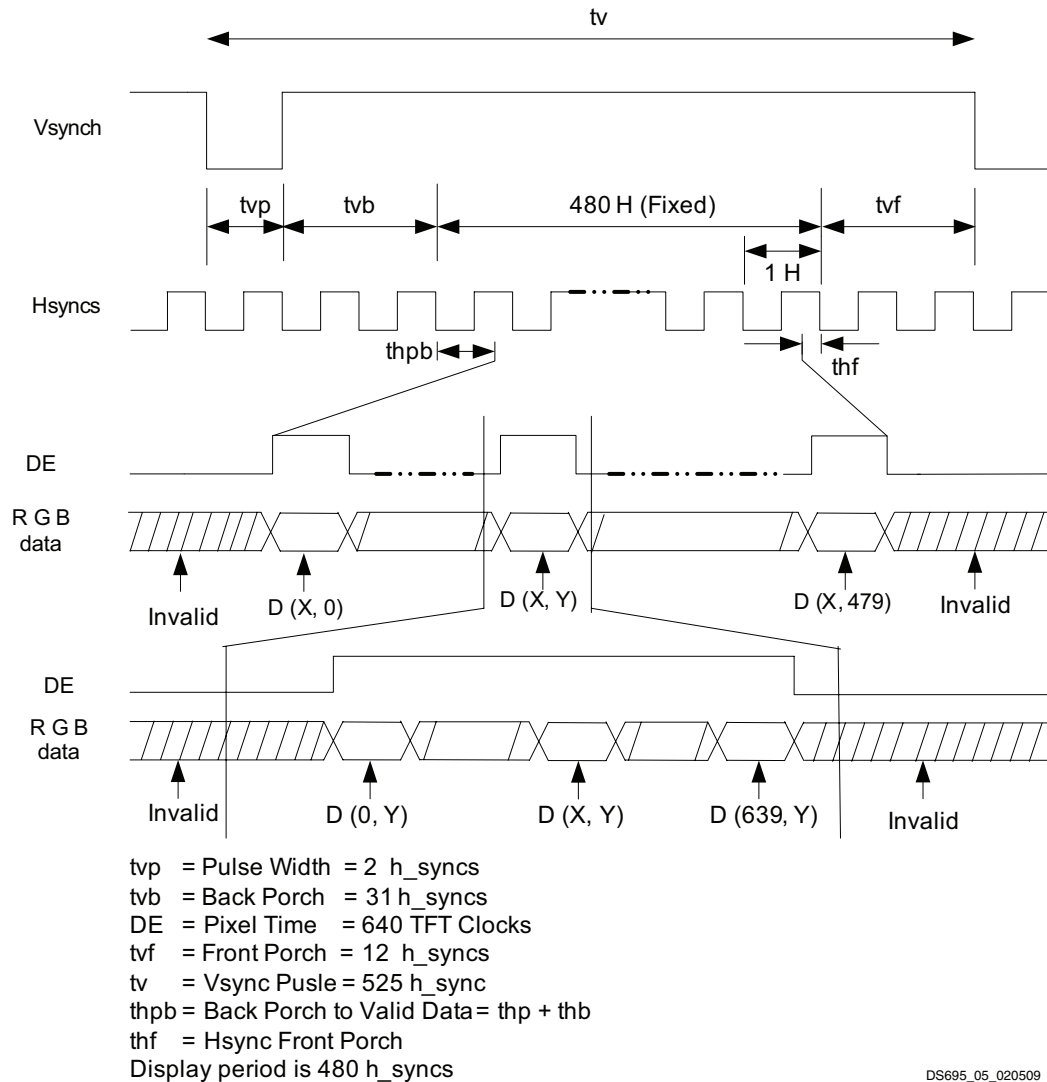


Figure 4: Horizontal Data

### Vsync Timing

The Vsync is active low signal and the complete time period of the Vsync is of 525 h\_syncs. Out of the 525 h\_syncs, the Vsync pulse period is of 2 h\_syncs, the active display period is of 480 h\_syncs, the back porch period is of 31 h\_syncs and the front porch period is of 12 h\_syncs. The Vsync timing with respect to the Hsync is shown in [Figure 5](#).



DS695\_05\_020509

Figure 5: Vertical Data

### Video Memory

It is important to design the system so that there is a sufficient bandwidth available between the XPS TFT controller and the PLB memory device to meet the video bandwidth requirements of the TFT. Furthermore, there must be enough bandwidth available for rest of the system. If the bandwidth requirement of rest of the system is more, the TFT clock frequency can be reduced. However, reducing the TFT clock frequency also lowers the refresh rate of the screen. This may lead to a noticeable flicker on the screen if the TFT clock is too slow. The PLB master interface logic has the ability to skip reading a line of data if it fails to finish reading data from a previous line because of shortage of PLB bandwidth. This prevents the XPS TFT controller losing synchronization between the PLB and TFT interface logic. Note that extreme shortage of available bandwidth for the XPS TFT controller may cause the screen to appear unstable as stale lines of video data are displayed on the screen.

The video memory is expected to be arranged so that each RGB pixel is represented by a 32-bit word in memory. The video memory should be stored in a 2 MB region of memory consisting of 1024 data



words (1 word = 32 bits) per line by 512 lines per frame. Out of this 1024 x 512 memory space, only the first 640 columns and 480 rows are displayed on the screen.

For a given row (0 to 479) and column (0 to 639), the pixel color information is encoded as shown in [Table 4](#).

*Table 4: Pixel Color Encoding*

| Pixel Address  | Bits    | Description  |
|--|---------|--|
| TFT Base Address +<br>(4096 * row) +<br>(4 * column) | [0:7]   | Undefined  |
|  | [8:13]  | Red Pixel Data:<br>000000 = darkest → 111111 = brightest   |
|  | [14:15] | Undefined  |
|  | [16:21] | Green Pixel Data:<br>000000 = darkest → 111111 = brightest |
|  | [22:23] | Undefined  |
|  | [24:29] | Blue Pixel Data:<br>000000 = darkest → 111111 = brightest  |
|  | [30:31] | Undefined  |

## XPS TFT Controller I/O Signals

The XPS TFT controller I/O signals are listed and described in [Table 5](#).

*Table 5: XPS TFT Controller I/O Signal Description*

| Port                                | Signal Name                 | Interface | I/O | Initial State | Description                                    |
|-------------------------------------|-----------------------------|-----------|-----|---------------|--|
| <b>System Signals</b>               |                             |           |     |               |  |
| P1                                  | MPLB_Clk                    | System    | I   | -             | PLB master clock                               |
| P2                                  | MPLB_Rst                    | System    | I   | -             | PLB master reset                               |
| P3                                  | SPLB_Clk <sup>(1)</sup>     | System    | I   | -             | PLB slave clock                                |
| P4                                  | SPLB_Rst                    | System    | I   | -             | PLB slave reset                                |
| P5                                  | MD_error                    | System    | O   | 0             | Master error detection indicator (active high) |
| P6                                  | IP2INTC_Irpt                | System    | O   | 0             | Vsync Pulse Interrupt                          |
| <b>PLB Master Interface Signals</b> |                             |           |     |               |  |
| P7                                  | M_request                   | PLB       | O   | 0             | Master bus request                             |
| P8                                  | M_priority                  | PLB       | O   | 0             | Master bus request priority                    |
| P9                                  | M_buslock                   | PLB       | O   | 0             | Master bus lock                                |
| P10                                 | M_RNW                       | PLB       | O   | 0             | Master read not write                          |
| P11                                 | M_BE(0:[C_MPLB_DWIDTH/8]-1) | PLB       | O   | 0             | Master byte enables                            |
| P12                                 | M_Msize(0:1)                | PLB       | O   | 0             | Master data bus size                           |

Table 5: XPS TFT Controller I/O Signal Description (Cont.)

| Port                                       | Signal Name                    | Interface | I/O | Initial State | Description                                |
|--|--------------------------------|-----------|-----|---------------|--|
| P13  | M_size(0:3)                    | PLB       | O   | 0             | Master transfer size                       |
| P14  | M_type(0:2)                    | PLB       | O   | 0             | Master transfer type                       |
| P15  | M_ABus(0:31)                   | PLB       | O   | 0             | Master address bus                         |
| P16  | M_wrBurst                      | PLB       | O   | 0             | Master burst write transfer indicator      |
| P17  | M_rdBurst                      | PLB       | O   | 0             | Master read write transfer indicator       |
| P18  | M_wrDBus(0:C_MPLB_DWIDT H-1)   | PLB       | O   | 0             | Master write data bus                      |
| P19  | PLB_MSize(0:1)                 | PLB       | I   | -             | PLB master slave data bus port width       |
| P20  | PLB_MaddrAck                   | PLB       | I   | -             | PLB master address acknowledge             |
| P21  | PLB_Mrearbitrate               | PLB       | I   | -             | PLB master bus rearbitrate indicator       |
| P22  | PLB_MTimeout                   | PLB       | I   | -             | PLB master bus time out                    |
| P23  | PLB_MRdErr                     | PLB       | I   | -             | PLB master slave read error indicator      |
| P24  | PLB_MWrErr                     | PLB       | I   | -             | PLB master slave write error indicator     |
| P25  | PLB_MRdDBus(0:C_MPLB_DWIDTH-1) | PLB       | I   | -             | PLB master read data bus                   |
| P26  | PLB_MRdDAck                    | PLB       | I   | -             | PLB master read data acknowledge           |
| P27  | PLB_MWrDAck                    | PLB       | I   | -             | PLB master write data acknowledge          |
| P28  | PLB_RdBTerm                    | PLB       | I   | -             | PLB master terminate read burst indicator  |
| P29  | PLB_MWrBTerm                   | PLB       | I   | -             | PLB master terminate write burst indicator |
| <b>Unused PLB Master Interface Signals</b> |                                |           |     |               |  |
| P30  | M_TAttribute(0 to 15)          | PLB       | O   | 0             | Master transfer attribute                  |
| P31  | M_lockerr                      | PLB       | O   | 0             | Master lock error indicator                |
| P32  | M_abort                        | PLB       | O   | 0             | Master abort bus request indicator         |
| P33  | M_UABus(0:31))                 | PLB       | O   | 0             | Master upper address                       |
| P34  | PLB_MBusy                      | PLB       | I   | -             | PLB master busy signal                     |
| P35  | PLB_MIRQ                       | PLB       | I   | -             | PLB master interrupt indicator             |
| P36  | PLB_RdWdAddr(0:3)              | PLB       | I   | -             | PLB master read word address               |

**Table 5: XPS TFT Controller I/O Signal Description (Cont.)**

| Port                                      | Signal Name                              | Interface | I/O | Initial State | Description                                      |
|---|--|-----------|-----|---------------|--|
| <b>PLB Slave Interface Signals</b>        |  |           |     |               |  |
| P37                                       | PLB_ABus[0:<br>C_SPLB_AWIDTH - 1]        | PLB       | I   | -             | PLB address bus                                  |
| P38                                       | PLB_PAVValid                             | PLB       | I   | -             | PLB primary address valid                        |
| P39                                       | PLB_masterID[0:<br>C_SPLB_MID_WIDTH - 1] | PLB       | I   | -             | PLB current master identifier                    |
| P40                                       | PLB_RNW                                  | PLB       | I   | -             | PLB read not write                               |
| P41                                       | PLB_BE[0:<br>(C_SPLB_DWIDTH/8) - 1]      | PLB       | I   | -             | PLB byte enables                                 |
| P42                                       | PLB_size[0:3]                            | PLB       | I   | -             | PLB size of requested transfer                   |
| P43                                       | PLB_type[0:2]                            | PLB       | I   | -             | PLB transfer type                                |
| P44                                       | PLB_wrDBus[0:<br>C_SPLB_DWIDTH - 1]      | PLB       | I   | -             | PLB write data bus                               |
| P45                                       | SI_addrAck                               | PLB       | O   | 0             | Slave address acknowledge                        |
| P46                                       | SI_SSize[0:1]                            | PLB       | O   | 0             | Slave data bus size                              |
| P47                                       | SI_wait                                  | PLB       | O   | 0             | Slave wait                                       |
| P48                                       | SI_rearbitrate                           | PLB       | O   | 0             | Slave bus rearbitrate                            |
| P49                                       | SI_wrDAck                                | PLB       | O   | 0             | Slave write data acknowledge                     |
| P50                                       | SI_wrComp                                | PLB       | O   | 0             | Slave write transfer complete                    |
| P51                                       | SI_rdDBus[0:<br>C_SPLB_DWIDTH - 1]       | PLB       | O   | 0             | Slave read data bus                              |
| P52                                       | SI_rdDAck                                | PLB       | O   | 0             | Slave read data acknowledge                      |
| P53                                       | SI_rdComp                                | PLB       | O   | 0             | Slave read transfer complete                     |
| P54                                       | SI_MBusy[0:<br>C_SPLB_NUM_MASTERS - 1]   | PLB       | O   | 0             | Slave busy                                       |
| P55                                       | SI_MWrErr[0:<br>C_SPLB_NUM_MASTERS - 1]  | PLB       | O   | 0             | Slave write error                                |
| P56                                       | SI_MRdErr[0:<br>C_SPLB_NUM_MASTERS - 1]  | PLB       | O   | 0             | Slave read error                                 |
| <b>Unused PLB Slave Interface Signals</b> |  |           |     |               |  |
| P57                                       | PLB_UABus[0: 31]                         | PLB       | I   | -             | PLB upper address bits                           |
| P58                                       | PLB_SAVValid                             | PLB       | I   | -             | PLB secondary address valid                      |
| P59                                       | PLB_rdPrim                               | PLB       | I   | -             | PLB secondary to primary read request indicator  |
| P60                                       | PLB_wrPrim                               | PLB       | I   | -             | PLB secondary to primary write request indicator |
| P61                                       | PLB_abort                                | PLB       | I   | -             | PLB abort bus request                            |

Table 5: XPS TFT Controller I/O Signal Description (Cont.)

| Port                               | Signal Name                            | Interface | I/O | Initial State | Description                          |
|------------------------------------|--|-----------|-----|---------------|--------------------------------------|
| P62                                | PLB_busLock                            | PLB       | I   | -             | PLB bus lock                         |
| P63                                | PLB_MSize                              | PLB       | I   | -             | PLB data bus width indicator         |
| P64                                | PLB_lockErr                            | PLB       | I   | -             | PLB lock error                       |
| P65                                | PLB_wrBurst                            | PLB       | I   | -             | PLB burst write transfer             |
| P66                                | PLB_rdBurst                            | PLB       | I   | -             | PLB burst read transfer              |
| P67                                | PLB_wrPendReq                          | PLB       | I   | -             | PLB pending bus write request        |
| P68                                | PLB_rdPendReq                          | PLB       | I   | -             | PLB pending bus read request         |
| P69                                | PLB_wrPendPri[0:1]                     | PLB       | I   | -             | PLB pending write request priority   |
| P70                                | PLB_rdPendPri[0:1]                     | PLB       | I   | -             | PLB pending read request priority    |
| P71                                | PLB_reqPri[0:1]                        | PLB       | I   | -             | PLB current request priority         |
| P72                                | PLB_TAttribute[0:15]                   | PLB       | I   | -             | PLB transfer attribute               |
| P73                                | SI_wrBTerm                             | PLB       | O   | 0             | Slave terminate write burst transfer |
| P74                                | SI_rdWdAddr[0:3]                       | PLB       | O   | 0             | Slave read word address              |
| P75                                | SI_rdBTerm                             | PLB       | O   | 0             | Slave terminate read burst transfer  |
| P76                                | SI_MIRQ[0:<br>C_SPLB_NUM_MASTERS - 1]  | PLB       | O   | 0             | Master interrupt request             |
| <b>DCR Slave Interface Signals</b> |  |           |     |               |                                      |
| P77                                | DCR_Clk <sup>(1)</sup>                 | DCR       | I   | -             | DCR clock                            |
| P78                                | DCR_Rst                                | DCR       | I   | -             | DCR reset                            |
| P79                                | DCR_Read                               | DCR       | I   | -             | DCR read request from DCR master     |
| P80                                | DCR_Write                              | DCR       | I   | -             | DCR write request from DCR master    |
| P81                                | DCR_ABus[0 :<br>C_SDCR_AWIDTH-1]       | DCR       | I   | -             | DCR address bus from DCR master      |
| P82                                | DCR_SI_DBus[0 :<br>C_SDCR_DWIDTH-1]    | DCR       | I   | -             | DCR slave data bus from DCR master   |
| P83                                | SI_DCR_DBusout[0 :<br>C_SDCR_DWIDTH-1] | DCR       | O   | 0             | Slave DCR data bus out               |
| P84                                | SI_dcrAck                              | DCR       | O   | 0             | Slave DCR acknowledge                |
| <b>TFT Interface Signals</b>       |  |           |     |               |                                      |
| P85                                | SYS_TFT_Clk                            | TFT       | I   | -             | TFT clock input                      |
| P86                                | TFT_HSYNC                              | TFT       | O   | 1             | Horizontal Sync (Active Low)         |

**Table 5: XPS TFT Controller I/O Signal Description (Cont.)**

| Port | Signal Name        | Interface | I/O | Initial State | Description                                       |
|------|--------------------|-----------|-----|---------------|---|
| P87  | TFT_VSYNC          | TFT       | O   | 1             | Vertical Sync (Active Low)                        |
| P88  | TFT_DE             | TFT       | O   | 0             | Data enable                                       |
| P89  | TFT_DPS            | TFT       | O   | 0             | TFT Display scan                                  |
| P90  | TFT_VGA_CLK        | TFT-VGA   | O   | 0             | TFT VGA clock <sup>(2)</sup>                      |
| P91  | TFT_VGA_R[5:0]     | TFT-VGA   | O   | 0             | TFT VGA Red pixel data <sup>(2)</sup>             |
| P92  | TFT_VGA_G[5:0]     | TFT-VGA   | O   | 0             | TFT VGA Green pixel data <sup>(2)</sup>           |
| P93  | TFT_VGA_B[5:0]     | TFT-VGA   | O   | 0             | TFT VGA Blue pixel data <sup>(2)</sup>            |
| P94  | TFT_DVI_CLK_P      | TFT-DVI   | O   | 0             | Differential TFT DVI clock <sup>(3)</sup>         |
| P95  | TFT_DVI_CLK_N      | TFT-DVI   | O   | 0             | Differential TFT DVI clock <sup>(3)</sup>         |
| P96  | TFT_DVI_DATA[11:0] | TFT-DVI   | O   | 0             | TFT DVI data <sup>(3)</sup>                       |
| P97  | TFT_IIC_SCL_O      | TFT-DVI   | O   | 0             | I2C output clock to Chrontel chip <sup>(4)</sup>  |
| P98  | TFT_IIC_SCL_I      | TFT-DVI   | I   | -             | I2C input clock from Chrontel chip <sup>(4)</sup> |
| P99  | TFT_IIC_SCL_T      | TFT-DVI   | O   | 1             | 3-state control for I2C clock <sup>(4)</sup>      |
| P100 | TFT_IIC_SDA_O      | TFT-DVI   | O   | 0             | I2C output data to Chrontel chip <sup>(4)</sup>   |
| P101 | TFT_IIC_SDA_I      | TFT-DVI   | I   | -             | I2C input data from Chrontel chip <sup>(4)</sup>  |
| P102 | TFT_IIC_SDA_T      | TFT-DVI   | O   | 1             | 3-state control for I2C data <sup>(4)</sup>       |

**Notes:**

1. This controller supports clock ratio of 1:1 or 1:2 only for slave interface clock(SPLB\_Clk/DCR\_Clk) and master interface clock(MPLB\_Clk).
2. VGA interface signals.
3. DVI interface signals.
4. I2C signals are used to configure Chrontel Video Encoder chip. These ports are active when DVI interface is selected.

## XPS TFT Controller Design Parameters

To allow the user to create a XPS TFT controller that is uniquely tailored for the user's system, certain features are parameterizable in the XPS TFT controller design. This allows the user to have a design that utilizes only the resources required by the system and runs at the best possible performance. The features that are parameterizable in the XPS TFT controller core are shown in [Table 6](#).

Table 6: XPS TFT Controller Design Parameters

| Generic                                | Feature/Description                                    | Parameter Name                         | Allowable Values   | Default Value        | VHDL Type        |
|--|--|--|--|----------------------|------------------|
| <b>XPS TFT Controller Parameter</b>    |  |  |  |                      |                  |
| G1                                     | Target FPGA family                                     | C_FAMILY                               | spartan3a,<br>aspartan3a,<br>spartan3,<br>aspartan3,<br>spartan3e,<br>aspartan3e,<br>spartan3adsp,<br>aspartan3adsp,<br>spartan6, virtex4,<br>qvirtex4,<br>qrvirtex4, virtex5,<br>virtex5fx, virtex6,<br>virtex6cx | virtex4              | string           |
| G2                                     | Base address of PLB attached Video memory              | C_DEFAULT_TFT_BASE_ADDR <sup>(1)</sup> | valid address  | 0xF0000000           | std_logic_vector |
| G3                                     | Controller Register access interface                   | C_DCR_SPLB_SLAVE_IF                    | 0 = DCR slave interface<br>1 = PLB slave interface   | 1                    | integer          |
| G4                                     | TFT interface selection                                | C_TFT_INTERFACE                        | 0 = VGA interface<br>1 = DVI interface   | 1                    | integer          |
| G5                                     | I2C Slave address of external Chrontel DVI transmitter | C_I2C_SLAVE_ADDR                       | Valid 7 bit I2C slave address  | "1110110"            | std_logic_vector |
| <b>DCR Interface Parameters</b>        |  |  |  |                      |                  |
| G6                                     | DCR Slave Base Address                                 | C_DCR_BASEADDR                         | Valid Address  | Valid 10-bit address | std_logic_vector |
| G7                                     | DCR Slave High Address                                 | C_DCR_HIGHADDR                         | Valid Address  | Valid 10-bit address | std_logic_vector |
| <b>PLB Master Interface Parameters</b> |  |  |  |                      |                  |
| G8                                     | Address bus width of PLB                               | C_MPLB_AWIDTH                          | 32   | 32                   | integer          |
| G9                                     | Data bus width of the PLB                              | C_MPLB_DWIDTH                          | 64, 128  | 64                   | integer          |

Table 6: XPS TFT Controller Design Parameters (Cont.)

| Generic                               | Feature/Description                            | Parameter Name        | Allowable Values   | Default Value       | VHDL Type        |
|---------------------------------------|--|-----------------------|--|---------------------|------------------|
| G10                                   | Data width of the PLB attached video memory    | C_MPLB_SMALLEST_SLAVE | 32, 64, 128  | 64                  | integer          |
| G11                                   | Internal native data width of master interface | C_MPLB_NATIVE_DWIDTH  | 64   | 64                  | integer          |
| <b>PLB Slave Interface Parameters</b> |  |                       |  |                     |                  |
| G12                                   | XPS TFT controller Base Address                | C_SPLB_BASEADDR       | Valid Address <sup>(3)</sup>                                     | None <sup>(2)</sup> | std_logic_vector |
| G13                                   | XPS TFT controller High Address                | C_SPLB_HIGHADDR       | Valid Address <sup>(3)</sup>                                     | None <sup>(2)</sup> | std_logic_vector |
| G14                                   | PLB slave interface address width              | C_SPLB_AWIDTH         | 32   | 32                  | integer          |
| G15                                   | PLB slave interface data width                 | C_SPLB_DWIDTH         | 32, 64, 128  | 32                  | integer          |
| G16                                   | Selects point-to-point or shared PLB topology  | C_SPLB_P2P            | 0 = Shared Bus Topology  | 0                   | integer          |
| G17                                   | PLB Master ID bus width                        | C_SPLB_MID_WIDTH      | $\log_2(\text{C\_SPLB\_NUM\_MASTERS})$ with a minimum value of 1 | 1                   | integer          |
| G18                                   | Number of PLB Masters                          | C_SPLB_NUM_MASTERS    | 1 - 16   | 1                   | integer          |
| G19                                   | Width of the internal slave data bus           | C_SPLB_NATIVE_DWIDTH  | 32   | 32                  | integer          |

**Notes:**

1. C\_DEFAULT\_TFT\_BASE\_ADDR specifies the base address of PLB attached video memory. This base address of video memory must be aligned on a 2MB boundary (i.e. only upper 11 bits are valid, the remaining address bits must be always '0'). The controller will only use 11 MSB of this base address to read data from the video memory.
2. No default value will be specified to insure that the actual value is set, i.e., if the value is not set, a compiler error will be generated.
3. C\_SPLB\_BASEADDR must be a multiple of the range size, where the range size is C\_SPLB\_HIGHADDR - C\_SPLB\_BASEADDR + 1 and must be a power of two. The range size must be large enough to accommodate all of the registers.

### Allowable Parameter Combinations

The address-range size specified by C\_SPLB\_BASEADDR and C\_SPLB\_HIGHADDR must be a power of 2, and must be at least 0x10.

The address specified by C\_DEFAULT\_TFT\_BASE\_ADDR must be aligned on a 2MB boundary. Only 11 MSB bits should have valid address, the remaining address bits must be always '0'.

The PLB slave interface is only included in the design if C\_DCR\_SPLB\_SLAVE\_IF is set to 1. When C\_DCR\_SPLB\_SLAVE\_IF = 0, DCR slave interface is included in the design and all the PLB ports are unused.

## Optimal System Settings

It is recommended to have separate buses for the video memory access from the core and the rest of the system. This will have sufficient bandwidth available between XPS TFT controller and PLB memory device.

The native data width of XPS TFT controller is fixed to 64-bits. Optimal performance will be achieved when the video memory interface width is greater than or equal to native data width of PLB master interface ( $C\_MPLB\_SMALLEST\_SLAVE \geq C\_MPLB\_NATIVE\_DWIDTH$ ).

## XPS TFT Controller Parameter - Port Dependencies

The dependencies between the XPS TFT controller core design parameters and I/O signals are described in [Table 7](#). In addition, when certain features are parameterized out of the design, the related logic will no longer be a part of the design. The unused input signals and related output signals are set to a specified value.

Table 7: XPS TFT Controller Design Parameter - Port Dependencies

| Generic or Port          | Name                              | Affects            | Depends | Relationship Description  |
|--------------------------|-----------------------------------|--------------------|---------|---|
| <b>Design Parameters</b> |                                   |                    |         |   |
| G3                       | C_DCR_SPLB_SLAVE_IF               | P36 - P83          | -       | Affect DCR/PLB interface ports. If C_DCR_SPLB_SLAVE_IF = 1, all DCR ports are inactive. If C_DCR_SPLB_SLAVE_IF = 0, all PLB ports are inactive. |
| G4                       | C_TFT_INTERFACE                   | P89 - P101         | -       | Affects TFT interface ports. If C_TFT_INTERFACE = 1, all VGA ports are tied to '0'. If C_TFT_INTERFACE = 0, all DVI ports are tied to '0'.      |
| G5                       | C_I2C_SLAVE_ADDR                  | -                  | G4      | Depends on C_TFT_INTERFACE. Required only when DVI interface is selected.   |
| G9                       | C_MPLB_DWIDTH                     | P10, P17, P24      | -       | Affects the number of bits in PLB master data bus   |
| G13                      | C_SPLB_AWIDTH                     | P36                | -       | Affects number of bits in address bus   |
| G14                      | C_SPLB_DWIDTH                     | P40, P43, P50      | -       | Affects number of bits in slave data bus  |
| G16                      | C_SPLB_MID_WIDTH                  | P38                | G18     | Affects the width of current master identifier signals and depends on $\log_2(C\_SPLB\_NUM\_MASTERS)$ with a minimum value of 1                 |
| G17                      | C_SPLB_NUM_MASTERS                | P53, P54, P55, P75 | -       | Affects the width of busy and error signals   |
| <b>I/O Signals</b>       |                                   |                    |         |   |
| P10                      | M_BE[0:<br>(C_MPLB_DWIDTH/8) - 1] | -                  | G9      | Width varies with the size of the PLB master data bus   |
| P17                      | M_wrDBus[0:<br>C_MPLB_DWIDTH - 1] | -                  | G9      | Width varies with the size of the PLB master data bus   |



**Table 7: XPS TFT Controller Design Parameter - Port Dependencies (Cont.)**

| <b>Generic or Port</b> | <b>Name</b>                                | <b>Affects</b> | <b>Depends</b> | <b>Relationship Description</b>                             |
|------------------------|--|----------------|----------------|---|
| P24                    | PLB_MRdDBus[0:<br>C_MPLB_DWIDTH - 1]       | -              | G9             | Width varies with the size of the PLB master data bus       |
| P36                    | PLB_ABus[0:<br>C_SPLB_AWIDTH - 1]          | -              | G14            | Width varies with the size of the PLB address bus           |
| P38                    | PLB_masterID[0:<br>C_SPLB_MID_WIDTH - 1]   | -              | G17            | Width varies with the size of the PLB master identifier bus |
| P40                    | PLB_BE[0:<br>(C_SPLB_DWIDTH/8)-1]          | -              | G15            | Width varies with the size of the PLB slave data bus        |
| P43                    | PLB_wrDBus[0:<br>C_SPLB_DWIDTH - 1]        | -              | G15            | Width varies with the size of the PLB slave data bus        |
| P50                    | SI_rdDBus[0:<br>C_SPLB_DWIDTH - 1]         | -              | G15            | Width varies with the size of the PLB slave data bus        |
| P53                    | SI_MBusy[0:<br>C_SPLB_NUM_MASTERS<br>- 1]  | -              | G18            | Width varies with the number of PLB masters                 |
| P54                    | SI_MWrErr[0:<br>C_SPLB_NUM_MASTERS<br>- 1] | -              | G18            | Width varies with the number of PLB masters                 |
| P55                    | SI_MRdErr[0:<br>C_SPLB_NUM_MASTERS<br>- 1] | -              | G18            | Width varies with the number of PLB masters                 |
| P75                    | SI_MIRQ[0:<br>C_SPLB_NUM_MASTERS<br>- 1]   | -              | G18            | Width varies with the number of PLB masters                 |
| P36 -<br>P75           | PLB Slave Interface ports                  |                | G3             | Ports are unused when<br>C_DCR_SPLB_SLAVE_IF = 0            |
| P76 -<br>P82           | DCR Interface ports                        |                | G3             | Ports are unused when<br>C_DCR_SPLB_SLAVE_IF = 1            |
| P88                    | TFT_VGA_CLK                                | -              | G4             | Port tied to '0' when<br>C_TFT_INTERFACE = 1                |
| P89                    | TFT_VGA_R                                  | -              | G4             | Ports tied to '0' when<br>C_TFT_INTERFACE = 1               |
| P90                    | TFT_VGA_G                                  | -              | G4             | Ports tied to '0' when<br>C_TFT_INTERFACE = 1               |
| P91                    | TFT_VGA_B                                  | -              | G4             | Ports tied to '0' when<br>C_TFT_INTERFACE = 1               |
| P92                    | TFT_DVI_CLK_P                              | -              | G4             | Port tied to '0' when<br>C_TFT_INTERFACE = 0                |
| P93                    | TFT_DVI_CLK_N                              | -              | G4             | Port tied to '0' when<br>C_TFT_INTERFACE = 0                |
| P94                    | TFT_DVI_DATA                               | -              | G4             | Ports tied to '0' when<br>C_TFT_INTERFACE = 0               |

Table 7: XPS TFT Controller Design Parameter - Port Dependencies (Cont.)

| Generic or Port | Name          | Affects | Depends | Relationship Description                  |
|-----------------|---------------|---------|---------|---|
| P95             | TFT_IIC_SCL_O | -       | G4      | Port tied to '0' when C_TFT_INTERFACE = 0 |
| P96             | TFT_IIC_SCL_I | -       | G4      | Port is un-used when C_TFT_INTERFACE = 0  |
| P97             | TFT_IIC_SCL_T | -       | G4      | Port tied to '0' when C_TFT_INTERFACE = 0 |
| P98             | TFT_IIC_SDA_O | -       | G4      | Port tied to '0' when C_TFT_INTERFACE = 0 |
| P99             | TFT_IIC_SDA_I | -       | G4      | Port is un-used when C_TFT_INTERFACE = 0  |
| P100            | TFT_IIC_SDA_T | -       | G4      | Port tied to '0' when C_TFT_INTERFACE = 0 |

## XPS TFT Controller Register Description

There are four internal registers available in the XPS TFT controller design. These registers can be accessed through either PLB slave interface or DCR slave interface based on the parameter setting C\_DCR\_SPLB\_SLAVE\_IF. The memory map of the XPS TFT controller design is determined by setting the C\_SPLB\_BASEADDR/C\_DCR\_BASEADDR parameter. The internal registers of the XPS TFT controller are at a fixed offset from the base address on 32-bit boundary. Writing into the reserved registers has no effect. Reading from the reserved registers returns zero. All registers are defined for 32-bit access only. When the PLB slave interface is selected, any partial word write access (byte, half-word) has no effect on the registers and any partial word read access (byte, half-word) returns zero. All the partial access to the core register returns bus error. The XPS TFT controller internal registers and their offset for the PLB interface and the DCR interface are listed in [Table 8](#) and [Table 9](#).

Table 8: XPS TFT Controller Internal Registers access through PLB

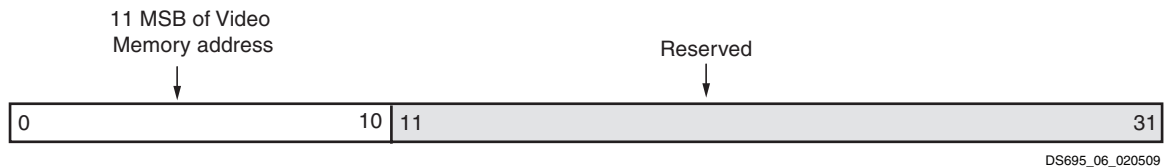
| Base Address + Offset (hex) | Register Name | Access     | Default Value (hex)     | Description  |
|-----------------------------|---------------|------------|-------------------------|--|
| C_SPLB_BASEADDR + 0         | AR            | Read/Write | C_DEFAULT_TFT_BASE_ADDR | TFT address register which specifies the base address of the video memory from which the controller fetches the data |
| C_SPLB_BASEADDR + 4         | CR            | Read/Write | 0x1                     | TFT control register   |
| C_SPLB_BASEADDR + 8         | IESR          | Read/Write | 0x0                     | Vsync interrupt enable and status register.  |
| C_SPLB_BASEADDR + C         | Reserved      | NA         | NA                      | Reserved for future use  |

**Table 9: XPS TFT Controller Internal Registers access through DCR**

| Base Address + Offset (hex) | Register Name | Access     | Default Value (hex)     | Description  |
|-----------------------------|---------------|------------|-------------------------|--|
| C_DCR_BASEADDR + 0          | AR            | Read/Write | C_DEFAULT_TFT_BASE_ADDR | TFT address register which specifies the base address of the video memory from which the controller fetches the data |
| C_DCR_BASEADDR + 1          | CR            | Read/Write | 0x1                     | TFT control register   |
| C_DCR_BASEADDR + 2          | IESR          | Read/Write | 0x0                     | Vsync interrupt enable and status register.  |
| C_DCR_BASEADDR + 3          | Reserved      | NA         | NA                      | Reserved for future use  |

### Address Register (AR)

TFT Base Address Register specifies the upper 11-bits of base address of the video memory. This is the address of PLB accessible memory device that acts as a video memory. This address must be aligned on a 2MB boundary (i.e. only upper 11 bits are writable, the remaining address bits are always '0') as shown in [Figure 6](#) and described in [Table 10](#).


**Figure 6: Address Register**
**Table 10: Address Register Description**

| Bits    | Name             | Core Access | Reset Value                   | Description   |
|---------|------------------|-------------|-------------------------------|---|
| [0:10]  | TFT base address | R/W         | C_DEFAULT_TFT_BASE_ADDR[0:10] | Specifies the base address of the video memory from which the controller fetched the data |
| [11:31] | Reserved         | N/A         | N/A                           | Reserved  |

### Control Register (CR)

TFT Control Register contains the control bits to configure the controller for TFT scanning mode and TFT display on/off. Writing '0' in TFT display enable bit resets the TFT controller. In the reset state, controller stops requesting data from the video memory by applying reset to the Master Interface

Module and set the Hsync and Vsync to their default value causing the display to enter in sleep mode. The bit assignment in the TFT control register is shown in **Figure 7** and described in **Table 11**.

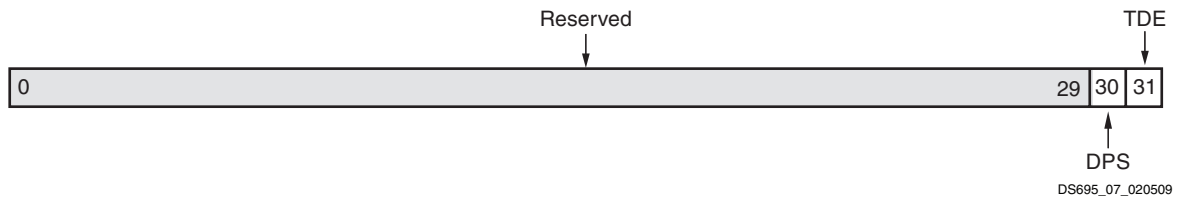


Figure 7: Control Register

Table 11: Control Register description

| Bits   | Name     | Core Access | Reset Value | Description   |
|--------|----------|-------------|-------------|---|
| [0:29] | Reserved | N/A         | N/A         | Reserved  |
| [30]   | DPS      | R/W         | 0           | Display Scan Control Bit<br>0 = Set DPS output bit to 0. This sets the display to use normal scan direction.<br>1 = Set DPS output bit to 1. This sets the display to use reverse scan direction (rotates screen 180 degrees).      |
| [31]   | TDE      | R/W         | 1           | TFT Display Enable Bit<br>0 = Disable TFT display. This resets the TFT controller and stops Vsync/Hsync signals causing display to go in sleep mode.<br>1 = Enable TFT display. This causes the TFT controller to operate normally. |

**Interrupt Enable and Status Register (IESR)**

TFT Interrupt Enable and Status register is a 32-bit read/write register. This register contains Vsync interrupt enable bit and the status bit. If Vsync interrupt is enabled, core generates interrupt for Vsyn pulse every frame. For every rising edge of Vsync pulse, core set status bit to indicate that core has displayed the current frame completely and accepted the new address from the AR. This status bit gets cleared for every write access to the AR. The bit assignment in the IESR is shown in **Figure 8** and described in **Table 12**.

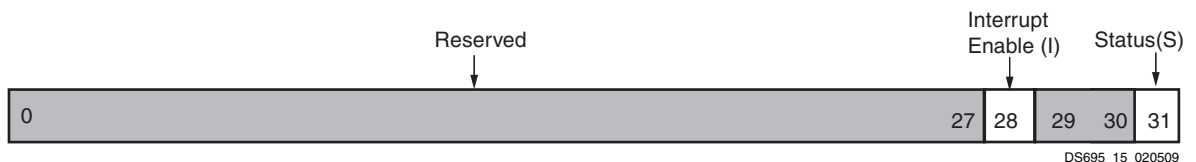


Figure 8: Interrupt Enable and Status Register

Table 12: Interrupt Enable and Status Register description

| Bits    | Name             | Core Access | Reset Value | Description  |
|---------|------------------|-------------|-------------|--|
| [0:27]  | Reserved         | N/A         | N/A         | Reserved   |
| [28]    | Interrupt Enable | R/W         | 0           | Vsync Interrupt Enable<br>0 = Disable Vsync pulse interrupt.<br>1 = Enable Vsync pulse interrupt.  |
| [29:30] | Reserved         | N/A         | N/A         | Reserved   |
| [31]    | Status           | R/W         | 0           | Vsync and address latch status bit<br>0 = Core is displaying current frame.<br>1 = Vsync pulse is active. Also indicate that previous frame is displayed completely and core has accepted new address from the AR. |

## XPS TFT Controller Timing Diagrams

### XPS TFT Master Burst Read on PLB attached Memory

The XPS TFT burst read transaction on PLB are shown in [Figure 9](#).

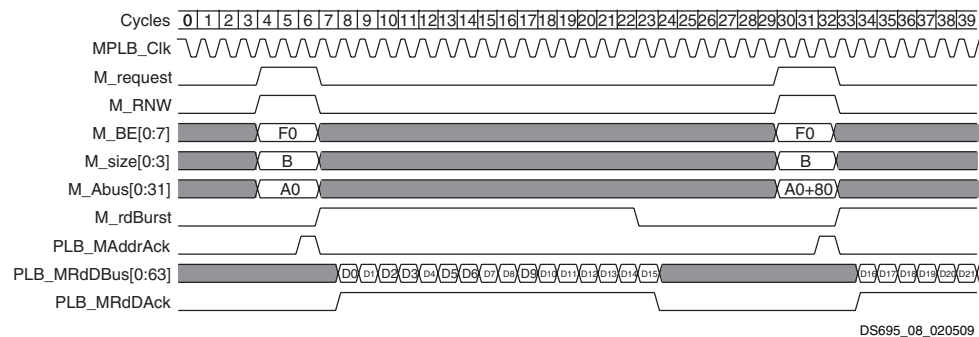


Figure 9: XPS TFT Burst Read Transaction on PLB

### XPS TFT Register Read/Write through PLB slave interface

[Figure 10](#) shows XPS TFT controller register access through PLB slave interface.

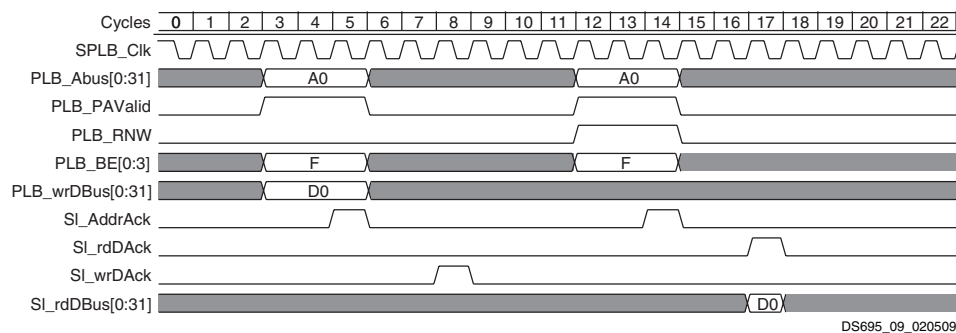


Figure 10: XPS TFT Register Read/Write Through PLB Slave Interface

## XPS TFT Register Read/Write through DCR slave interface

Figure 11 shows XPS TFT controller register access through DCR slave interface.

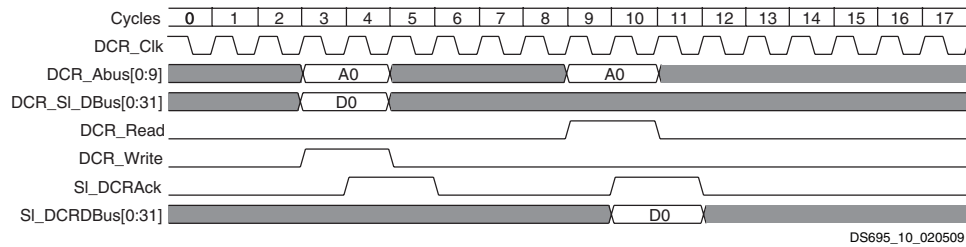


Figure 11: XPS TFT Register Read/Write Through DCR Slave Interface

## XPS TFT Use Cases

The XPS TFT controller system can be build for different use cases based on the processor interface and the core slave interface. Following are the uses cases for XPS TFT controller.

- Standard PowerPC® processor system with PLB slave interface (Figure 12)
- Standard PowerPC processor system with DCR slave interface (Figure 13)
- Microblaze™ processor system with DCR slave interface (Figure 14)
- PowerPC processor system with separate PLB bus for XPS TFT master and slave interface (Figure 15).

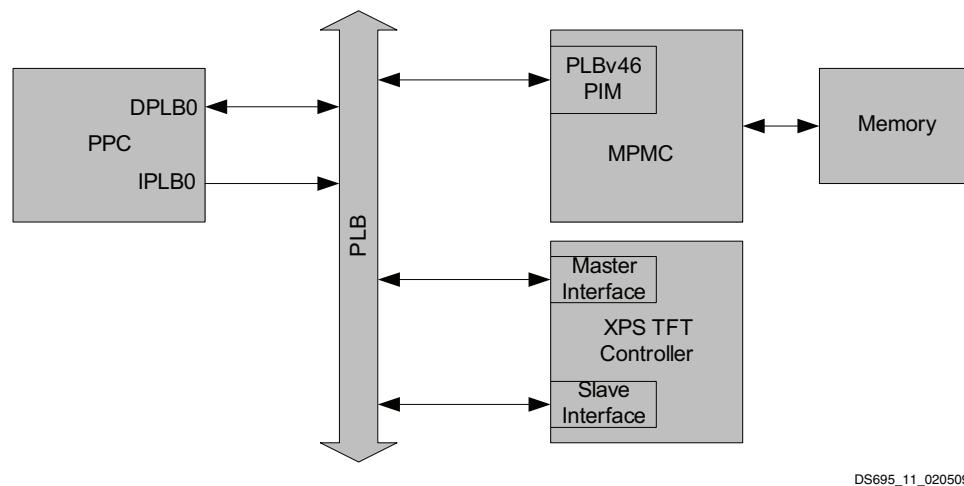
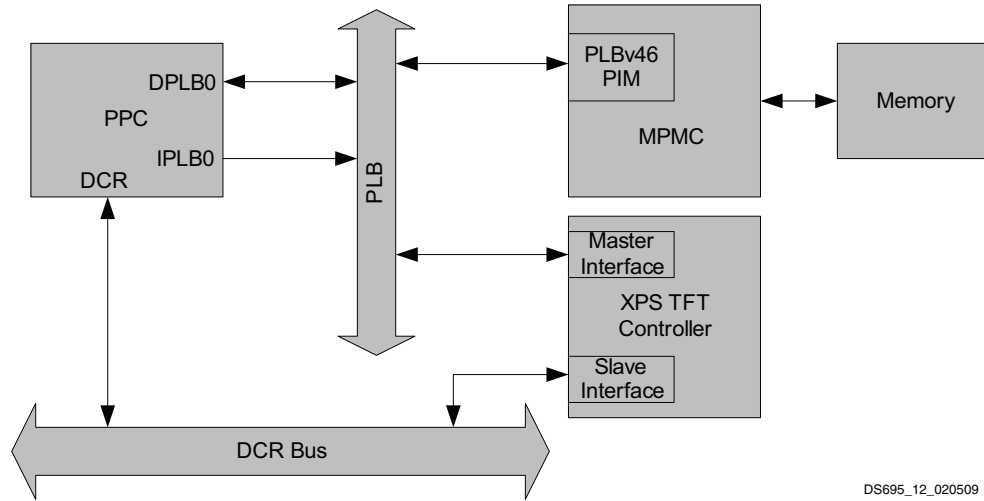
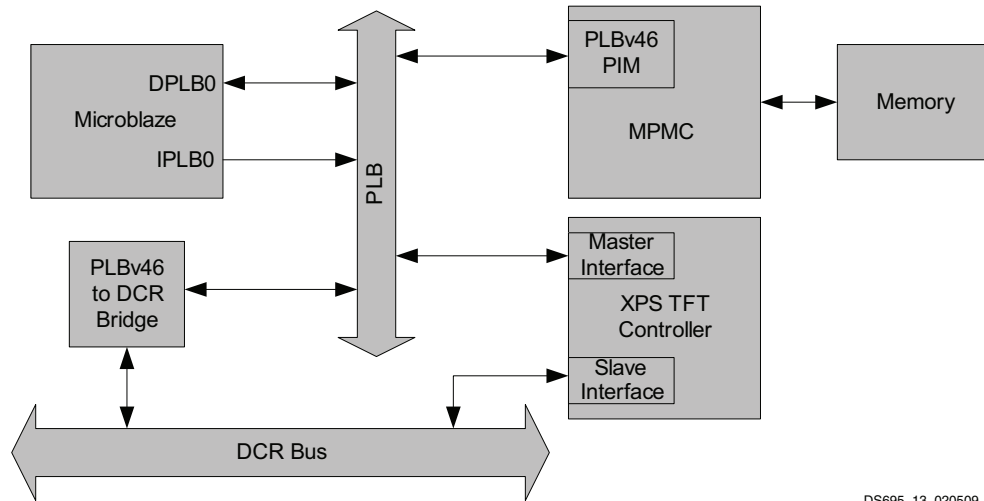


Figure 12: XPS TFT PowerPC Processor System with PLB Slave Interface



DS695\_12\_020509

Figure 13: XPS TFT PowerPC Processor System with DCR Slave Interface



DS695\_13\_020509

Figure 14: Microblaze System with DCR Slave Interface

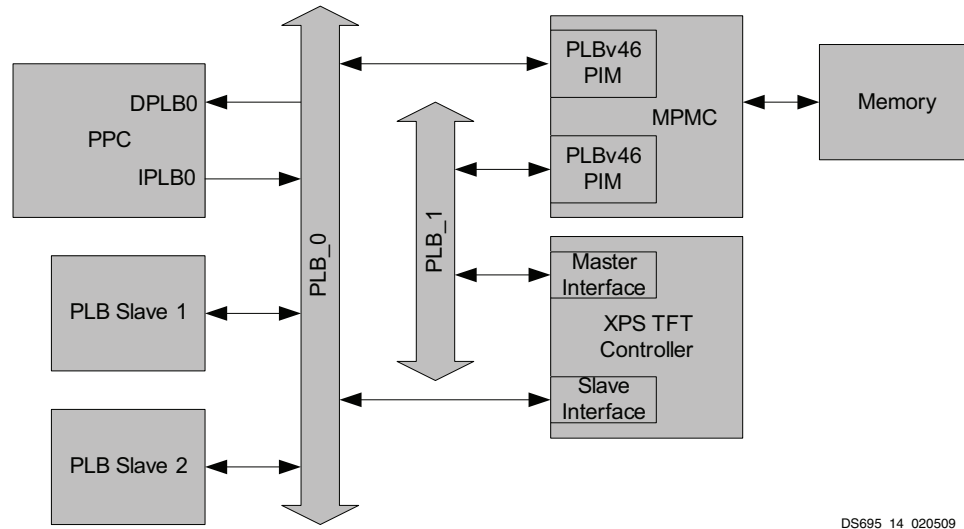


Figure 15: PowerPC Processor System with Separate PLB Buses for XPS TFT Master and Slave Interface

## Design Implementation

### Target Technology

The target technology is an FPGA listed in the **Supported Device Family** field of the LogiCORE Facts Table.

### Device Utilization and Performance Benchmarks

Since the XPS TFT controller core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When the XPS TFT controller core is combined with other designs in the system, the utilization of FPGA resources and timing of the XPS TFT controller design will vary from the results reported here.

The XPS TFT controller resource utilization for various parameter combinations measured with Virtex-4 FPGA as the target device are detailed in **Table 13**.

Table 13: Performance and Resource Utilization Benchmarks on the Virtex-4 FPGA (xc4vlx25-ff668-10)

| Parameter Values    |                 | Device Resources |                  |      | Performance            |
|---------------------|-----------------|------------------|------------------|------|------------------------|
| C_DCR_SPLB_SLAVE_IF | C_TFT_INTERFACE | Slices           | Slice Flip-Flops | LUTs | F <sub>MAX</sub> (MHz) |
| 0                   | 0               | 410              | 414              | 544  | 143                    |
| 0                   | 1               | 611              | 498              | 660  | 139                    |
| 1                   | 0               | 514              | 464              | 543  | 139                    |
| 1                   | 1               | 628              | 546              | 660  | 140                    |



The XPS TFT controller resource utilization for various parameter combinations measured with Virtex-5 as the target device are detailed in [Table 14](#).

**Table 14: Performance and Resource Utilization Benchmarks on Virtex-5 FPGA (xc5vfx70-ff1136-1)**

| Parameter Values    |                 | Device Resources |                  |      | Performance            |
|---------------------|-----------------|------------------|------------------|------|------------------------|
| C_DCR_SPLB_SLAVE_IF | C_TFT_INTERFACE | Slices           | Slice Flip-Flops | LUTs | F <sub>MAX</sub> (MHz) |
| 0                   | 0               | 276              | 414              | 479  | 154                    |
| 0                   | 1               | 389              | 498              | 598  | 152                    |
| 1                   | 0               | 364              | 462              | 478  | 153                    |
| 1                   | 1               | 412              | 546              | 596  | 152                    |

The XPS TFT controller resource utilization for various parameter combinations measured with the Spartan-3 FPGA as the target device are detailed in [Table 15](#).

**Table 15: Performance and Resource Utilization Benchmarks on the Spartan-3 FPGA (xc3sd1800a-fg676-4)**

| Parameter Values    |                 | Device Resources |                  |      | Performance            |
|---------------------|-----------------|------------------|------------------|------|------------------------|
| C_DCR_SPLB_SLAVE_IF | C_TFT_INTERFACE | Slices           | Slice Flip-Flops | LUTs | F <sub>MAX</sub> (MHz) |
| 0                   | 0               | 521              | 411              | 504  | 102                    |
| 0                   | 1               | 591              | 495              | 609  | 102                    |
| 1                   | 0               | 495              | 459              | 504  | 102                    |
| 1                   | 1               | 617              | 543              | 609  | 102                    |

The XPS TFT controller resource utilization for various parameter combinations measured with the Virtex-6 FPGA as the target device are detailed in [Table 16](#).

**Table 16: Performance and Resource Utilization Benchmarks on Virtex-6 FPGA (xc6vix75ft-ff784-1)**

| Parameter Values    |                 | Device Resources |                  |      | Performance            |
|---------------------|-----------------|------------------|------------------|------|------------------------|
| C_DCR_SPLB_SLAVE_IF | C_TFT_INTERFACE | Slices           | Slice Flip-Flops | LUTs | F <sub>MAX</sub> (MHz) |
| 0                   | 0               | 192              | 500              | 537  | 160                    |
| 0                   | 1               | 202              | 567              | 639  | 160                    |
| 1                   | 0               | 232              | 514              | 585  | 160                    |
| 1                   | 1               | 224              | 581              | 709  | 160                    |

The XPS TFT controller resource utilization for various parameter combinations measured with the Spartan-6 FPGA as the target device are detailed in [Table 17](#).

**Table 17: Performance and Resource Utilization Benchmarks on the Spartan-6 FPGA (xc6slx16-csg324-2)**

| Parameter Values    |                 | Device Resources |                  |      | Performance            |
|---------------------|-----------------|------------------|------------------|------|------------------------|
| C_DCR_SPLB_SLAVE_IF | C_TFT_INTERFACE | Slices           | Slice Flip-Flops | LUTs | F <sub>MAX</sub> (MHz) |
| 0                   | 0               | 198              | 449              | 543  | 100                    |
| 0                   | 1               | 292              | 433              | 658  | 100                    |
| 1                   | 0               | 245              | 462              | 622  | 100                    |
| 1                   | 1               | 265              | 547              | 723  | 100                    |

## Specification Exceptions

This core is capable of configuring Chrontel CH-7301 chip only. If the system has video encoder chip other than Chrontel CH-7301, user must take care of configuring the chip.

## Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

## Reference Documents

1. [DS402](#) Xilinx Device Control Register Bus Design Specification
2. DS561 Xilinx PLBV46 Slave Single Design Specification
3. DS565 Xilinx PLBV46 Master Burst Design Specification
4. IBM CoreConnect 128-Bit Processor Local Bus, Architectural Specification (v4.6)
5. IBM CoreConnect 32-Bit Device Control Register Bus: Architecture Specification, ver 2.9
6. Chrontel CH-7301C DVI Transmitter Specification, ver 1.32
7. I2C bus specification , ver 2.1

## Revision History

| Date     | Version | Revision   |
|----------|---------|--|
| 07/07/08 | 1.0     | Initial Xilinx release.  |
| 7/21/08  | 1.1     | Added QPro Virtex-4 Hi-Rel and QPro Virtex-4 Rad Tolerant support.   |
| 4/24/09  | 1.2     | Replaced references to supported device families and tool name(s) with hyperlink to PDF file.                    |
| 9/16/09  | 1.3     | Updated to v2.00.a; added Performance and Resource Utilization table for Virtex-6 and Spartan-6; updated images. |

## Notice of Disclaimer

Xilinx is providing this product documentation, hereinafter "Information," to you "AS IS" with no warranty of any kind, express or implied. Xilinx makes no representation that the Information, or any particular implementation thereof, is free from any claims of infringement. You are responsible for obtaining any rights you may require for any implementation based on the Information. All specifications are subject to change without notice. XILINX EXPRESSLY DISCLAIMS ANY WARRANTY WHATSOEVER WITH RESPECT TO THE ADEQUACY OF THE INFORMATION OR ANY IMPLEMENTATION BASED THEREON, INCLUDING BUT NOT LIMITED TO ANY WARRANTIES OR REPRESENTATIONS THAT THIS IMPLEMENTATION IS FREE FROM CLAIMS OF INFRINGEMENT AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Except as stated herein, none of the Information may be copied, reproduced, distributed, republished, downloaded, displayed, posted, or transmitted in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx.