VIRTEX UltraSCALE+

Virtex UltraScale+ FPGAs

Programmable System Integration

- Up to 3.6M system logic cells
- Up to 8GB of HBM Gen2 integrated in-package
- Up to 500Mb of total on-chip integrated memory
- Integrated 100G Ethernet MAC with KR4-FEC and 150G Interlaken cores
- Integrated blocks for PCI Express® Gen 3x16

Increased System Performance

- 38 TOP/s DSP compute performance
- 1.6X fabric performance versus Virtex-7
- Up to 128 transceivers operating at 32.75Gb/s or 48 PAM4 transceivers operating at 58Gb/s to deliver multi-terabit systems
- 460GB/s HBM bandwidth, and 2,666Mb/s DDR4 in the mid-speed grade

BOM Cost Reduction

- UltraRAM for on-chip memory integration
- VCXO and fractional PLL integration reduce clocking component cost

Total Power Reduction

- Industry's Most Energy-Efficient Machine Learning Inference
- Voltage scaling options for performance and power
- Up to 60% lower power vs. 7 series FPGAs

XILINX ALL PROGRAMMABLE™

Industry-Leading performance-per-watt

Virtex® UltraScale+™ devices provide 3X system-level performance-per-watt compared to 7 series FPGAs, along with system integration and bandwidth for a wide range of applications such as 1+ Tb/s Data Center, Wired Communications, and Waveform Processing applications. With optional integrated high-bandwidth memory (HBM) or 58G PAM4 transceivers, the Virtex UltraScale+ family delivers a step-function increase in performance, bandwidth, and reduced latency for systems demanding massive data flow and packet processing. Based on the ASIC-class advantage of the UltraScale™ architecture, Virtex UltraScale+ devices are co-optimized with the Vivado® Design Suite and leverage the UltraFAST™ design methodology to accelerate time to market.

Re-architecting the core for massive bandwidth with the UltraScale architecture

The UltraScale+ families are based on the first architecture to span multiple nodes from planar through FinFET technologies, and from monolithic through 3D ICs. Xilinx UltraScale architecture provides diverse benefits and advantages to an array of markets and applications. The architecture combines enhancements in the CLB, a dramatic increase in device routing, revolutionary ASIC-like clocking, high-performance DSPs, memory interface PHYs, NRZ and optional PAM4, serial transceivers, and optional HBM. All UltraScale architecture-based FPGAs are capable of pushing the system performance-per-watt envelope, enabling breakthrough speeds with high utilization. High system performance and multiple power reduction innovations make the UltraScale architecture the logical choice for next-generation applications.

Building on the success of Xilinx's UltraScale Portfolio

The UltraScale+ family of FPGAs, 3D ICs and MPSoCs, combine new memory, 3D-on-3D and MPSoC technologies, delivering a generation ahead of value. To enable an even higher level of performance and integration, the UltraScale+ family also includes a new IP interconnect optimization technology, SmartConnect. Built upon Xilinx's UltraScale Architecture, they leverage a significant boost in performance-per-watt using 16nm FinFET+ 3D transistors from the #1 service foundry in the world, TSMC. Xilinx provides scalability and package migration for the lowest risk and the highest value programmable technology.

FEATURES OVERVIEW

16nm low power FinFET+ process technology from TSMC Industry leading process from the #1 service foundry delivers a step function increase in performance-per-watt	• Over 2X performance-per-watt over 7 series devices • The same scalable architecture and tools from Virtex UltraScale FPGAs
Integrated HBM (Gen2): the highest DRAM bandwidth available Up to 8GB in-package DRAM with 460GB/s bandwidth	• 10X higher memory bandwidth relative to discrete memory channels • 4X less power per bit vs. competing memory technologies • Built using proven, 3rd generation 3D IC technology
Enhanced DSP slices for diverse applications Enabling a massive jump in fixed-and floating-point performance for a variety of workloads	• Up to 21.2 TeraMACs (38 TOP/s) of DSP compute bandwidth • Double-precision floating point using 30% fewer resources • Complex fixed-point arithmetic in half the resources
Massive memory interface bandwidth reduction Next generation DDR and serial memory support	• DDR4 support of up to 2,666 Mb/s • Support for server-class DIMMs (8X capacity vs. Virtex-7) • Hybrid Memory Cube serial memory support of up to 30G
Massive I/O bandwidth including optional 58Gb/s PAM4 transceivers 4X greater serial bandwidth than Virtex-7 devices	• 16G, 28G, or 58G backplane support • 32.75G or 58G chip-to-chip and chip-to-optics support • High-Density I/O for smaller area and greater power efficiency
SmartConnect Technology System-wide interconnect optimization tools and IP	• Matches optimal AXI interconnect to the design • Automatic interface bridging • Additional 20-30% advantage in performance-per-watt
Next-generation routing, ASIC-like clocking, and enhanced fabric Enabling breakthrough speeds with high utilization	• Lower skew, faster performing clock networks • Up to one speed-grade advantage vs. comparable solutions • Efficient CLB use and placement for reduced interconnect delay
Integrated blocks for PCI Express® with cache coherent CCIX ports Complete end-to-end solution for multi-100G ports	• Gen3 x16 for 100G bandwidth per block • Expanded virtualization for data center applications • Cache coherent acceleration using CCIX ports
Integrated 100G Ethernet MAC and 150G Interlaken Cores ASIC-class cores for breakthrough performance in packet processing	• 60K-100K system logic cell savings per port • Up to 90% dynamic power savings vs. soft implementation • Built-in KR4 -FEC (Ethernet MAC) for optics error correction • Optional built-in KP4-FEC for PAM4 optics and backplanes
High-speed memory cascading Removes key bottlenecks in DSP and packet processing	• Eliminates fabric usage when building deep memories • Reduces routing congestion • Lowers dynamic power consumption
Up to 60% power savings over Virtex-7 devices Static- and dynamic-power optimizations at every level	• Optimal voltage tuning • Power-optimized transceivers and block RAM • More granular clock gating of logic fabric and block RAM
Step-function increase in 3D IC inter-die bandwidth Virtual monolithic design	• Registered inter-die routing lines enable >600 MHz • Abundant and flexible clocking
Next-generation security Enhanced features to protect IP and prevent tampering	• AES-GCM decryption, RSA-2048 authentication • DPA Countermeasures and permanent tamper penalty • Improved SEU performance