XILINX VIRTEX®-5 FPGAS

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			Virtex-5 LX FPGAs Optimized for High-Performance Logic (1.0V)							Virtex-5 LXT FPGAs Optimized for High-Performance Logic with Low-Power Serial Connectivity (1.0V)							
	Part Number		XC5VLX30	XC5VLX50	XC5VLX85	XC5VLX110	XC5VLX155	XC5VLX220	XC5VLX330	XC5VLX20T	XC5VLX30T	XC5VLX50T	XC5VLX85T	XC5VLX110T	XC5VLX155T	XC5VLX220T	XC5VLX330T
	EasyPath™ FPGA Cost Reduction Solutions[1]		—	—	XCE5VLX85	XCE5VLX110	XCE5VLX155	XCE5VLX220	XCE5VLX330	—	—	—	XCE5VLX85T	XCE5VLX110T	XCE5VLX155T	XCE5VLX220T	XCE5VLX330T
Logic Resources	Slices[2]		4,800	7,200	12,960	17,280	24,320	34,560	51,840	3,120	4,800	7,200	12,960	17,280	24,320	34,560	51,840
	Logic Cells[3]		30,720	46,080	82,944	110,592	155,648	221,184	331,776	19,968	30,720	46,080	82,944	110,592	155,648	221,184	331,776
	CLB Flip-Flops		19,200	28,800	51,840	69,120	97,280	138,240	207,360	12,480	19,200	28,800	51,840	69,120	97,280	138,240	207,360
Memory Resources	Maximum Distributed RAM (Kb)		320	480	840	1,120	1,640	2,280	3,420	210	320	480	840	1,120	1,640	2,280	3,420
	Block RAM/FIFO w/ECC (36 Kb each)		32	48	96	128	192	192	288	26	36	60	108	148	212	212	324
	Total Block RAM (Kb)		1,152	1,728	3,456	4,608	6,912	6,912	10,368	936	1,296	2,160	3,888	5,328	7,632	7,632	11,664
Clock Resources	Digital Clock Managers (DCM)		4	12	12	12	12	12	12	2	4	12	12	12	12	12	12
	Phase-Locked Loop (PLL)/PMCD		2	6	6	6	6	6	6	1	2	6	6	6	6	6	6
I/O Resources[4,5]	Maximum Single-Ended Pins		400	560	560	800	800	800	1,200	172	360	480	480	680	680	680	960
	Maximum Differential I/O Pairs		200	280	280	400	400	400	600	86	180	240	240	340	340	340	480
Embedded Hard IP Resources[6]	DSP48E Slices		32	48	48	64	128	128	192	24	32	48	48	64	128	128	192
	PowerPC® 440 Processor Blocks		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Endpoint Blocks for PCI Express®		—	—	—	—	—	—	—	1	1	1	1	1	1	1	1
	10/100/1000 Ethernet MAC Blocks		—	—	—	—	—	—	—	2	4	4	4	4	4	4	4
	RocketIO™ GTP Low-Power Transceivers		—	—	—	—	—	—	—	4	8	12	12	16	16	16	24
	RocketIO GTX High-Speed Transceivers		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Speed Grades	Commercial		-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2	-1, -2	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2
	Industrial		-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1
Configuration	Configuration Memory (Mb)		8.4	12.6	21.9	29.1	41.1	53.2	79.8	6.3	9.4	14.1	23.4	31.2	43.1	55.2	82.7
	Package[7]	Area	Available User I/O: SelectIO™ Interface Pins[4,5] (GTP/GTX Serial Transceivers)														
	FFA Packages (FF): Flip-chip, fine-pitch BGA (1.0 mm ball spacing)																
	FF324	19 x 19 mm	220	220													
	FF676	27 x 27 mm	400	440	440	440											
	FF1153	35 x 35 mm		560	560	800	800										
	FF1760	42.5 x 42.5 mm				800	800	800	1,200								
	FF323	19 x 19 mm								172 (4)	172 (4)						
	FF665	27 x 27 mm									360 (8)	360 (8)					
	FF1136	35 x 35 mm										480 (12)	480 (12)	640 (16)	640 (16)		
	FF1738	42.5 x 42.5 mm												680 (16)	680 (16)	680 (16)	960 (24)
	FF1156	35 x 35 mm															
	FF1759	42.5 x 42.5 mm															

XMP069 (v1.2)

Notes:
1. EasyPath FPGAs provide a conversion-free, low-risk path for volume production.
2. A single Virtex-5 FPGA CLB comprises two slices, each containing four 6-input LUTs and four flip-flops (twice the number found in a Virtex-4 FPGA slice), for a total of eight 6-input LUTs and eight flip-flops per CLB.
3. Virtex-5 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
4. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
5. Supported I/O standards include: HT, LVDS, LVDSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V, 1.5V, 1.8V), HSTL II (1.5V, 1.8V), HSTL III (1.5V, 1.8V), HSTL IV (1.5V, 1.8V), SSTL2 I, SSTL2 II, SSTL18 I, and SSTL18 II.
6. One System Monitor block is included in all devices.
7. All products are available Pb-free and RoHS-Compliant (FFG/FFV).

XILINX VIRTEX®-5 FPGAS

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			Virtex-5 SXT FPGAs Optimized for DSP with Low-Power Serial Connectivity (1.0V)				**Virtex-5 FXT FPGAs** Optimized for Embedded Processing with High-Speed Serial Connectivity (1.0V)					**Virtex-5 TXT FPGAs** Optimized for Ultra-High Bandwidth (1.0V)	
		Part Number	XC5VSX35T	XC5VSX50T	XC5VSX95T	XC5VSX240T	XC5VFX30T	XC5VFX70T	XC5VFX100T	XC5VFX130T	XC5VFX200T	XC5VTX150T	XC5VTX240T
		EasyPath™ FPGA Cost Reduction Solutions[1]	—	XCE5VSX50T	XCE5VSX95T	XCE5VSX240T	—	XCE5VFX70T	XCE5VFX100T	XCE5VFX130T	XCE5VFX200T	XCE5VTX150T	XCE5VTX240T
Logic Resources		Slices[2]	5,440	8,160	14,720	37,440	5,120	11,200	16,000	20,480	30,720	23,200	37,440
		Logic Cells[3]	34,816	52,224	94,208	239,616	32,768	71,680	102,400	131,072	196, 608	148,480	239,616
		CLB Flip-Flops	21,760	32,640	58,880	149,760	20,480	44,800	64,000	81,920	122,880	92,800	149,760
Memory Resources		Maximum Distributed RAM (Kb)	520	780	1,520	4,200	380	820	1,240	1,580	2,280	1,500	2,400
		Block RAM/FIFO w/ECC (36 Kb each)	84	132	244	516	68	148	228	298	456	228	324
		Total Block RAM (Kb)	3,024	4,752	8,784	18,576	2,448	5,328	8,208	10,728	16,416	8,208	11,664
Clock Resources		Digital Clock Managers (DCM)	4	12	12	12	4	12	12	12	12	12	12
		Phase-Locked Loop (PLL)/PMCD	2	6	6	6	2	6	6	6	6	6	6
I/O Resources[4,5]		Maximum Single-Ended Pins	360	480	640	960	360	640	680	840	960	680	680
		Maximum Differential I/O Pairs	180	240	320	480	180	320	340	420	480	340	340
Embedded Hard IP Resources[6]		DSP48E Slices	192	288	640	1,056	64	128	256	320	384	80	96
		PowerPC® 440 Processor Blocks	—	—	—	—	1	1	2	2	2	—	—
		Endpoint Blocks for PCI Express®	1	1	1	1	1	3	3	3	4	1	1
		10/100/1000 Ethernet MAC Blocks	4	4	4	4	4	4	4	6	8	4	4
		RocketIO™ GTP Low-Power Transceivers	8	12	16	24	—	—	—	—	—	—	—
		RocketIO GTX High-Speed Transceivers	—	—	—	—	8	16	16	20	24	40	48
Speed Grades		Commercial	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2	-1, -2
		Industrial	-1, -2	-1, -2	-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1, -2	-1, -2
Configuration		Configuration Memory (Mb)	13.4	20.0	35.8	79.7	13.6	27.1	39.4	49.3	70.9	43.4	65.8
	Package[7]	Area	Available User I/O: SelectIO™ Interface Pins [4, 5] (GTP/GTX Serial Transceivers)										
FFA Packages (FF): Flip-chip, fine-pitch BGA (1.0 mm ball spacing)													
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	FF323	19 x 19 mm											
	FF665	27 x 27 mm	360 (8)	360 (8)			360 (8)	360 (8)					
	FF1136	35 x 35 mm		480 (12)	640 (16)			640 (16)	640 (16)				
	FF1738	42.5 x 42.5 mm				960 (24)			680 (16)	840 (20)	960 (24)		
	FF1156	35 x 35 mm										360 (40)	
	FF1759	42.5 x 42.5 mm										680 (40)	680 (48)

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6. One System Monitor block included in all devices.

7. All products are available Pb-free and RoHS-Compliant (FFG/FFV).