Virtex®-7 FPGAs

XILINX.

			Optimized for Highest System Performance and Capacity (1.0V)											
	Part Number		XC7V585T	XC7V2000T	XC7VX330T	XC7VX415T	XC7VX485T	XC7VX550T	XC7VX690T	XC7VX980T	XC7VX1140T	XC7VH580T	XC7VH870T
	EasyPath™ Cost Reduction Solutions[1]		XCE7V585T	—	XCE7VX330T	XCE7VX415T	XCE7VX485T	XCE7VX550T	XCE7VX690T	XCE7VX980T	—	—	—
Logic Resources	Slices		91,050	305,400	51,000	64,400	75,900	86,600	108,300	153,000	178,000	90,700	136,900
	Logic Cells		582,720	1,954,560	326,400	412,160	485,760	554,240	693,120	979,200	1,139,200	580,480	876,160
	CLB Flip-Flops		728,400	2,443,200	408,000	515,200	607,200	692,800	866,400	1,224,000	1,424,000	725,600	1,095,200
Memory Resources	Maximum Distributed RAM (Kb)		6,938	21,550	4,388	6,525	8,175	8,725	10,888	13,838	17,700	8,850	13,275
	Block RAM/FIFO w/ ECC (36 Kb each)		795	1,292	750	880	1,030	1,180	1,470	1,500	1,880	940	1,410
	Total Block RAM (Kb)		28,620	46,512	27,000	31,680	37,080	42,480	52,920	54,000	67,680	33,840	50,760
Clocking	CMTs (1 MMCM + 1 PLL)		18	24	14	12	14	20	20	18	24	12	18
I/O Resources	Maximum Single-Ended I/O		850	1,200	700	600	700	600	1,000	900	1,100	600	300
	Maximum Differential I/O Pairs		408	576	336	288	336	288	480	432	528	288	144
Integrated IP Resources	DSP Slices		1,260	2,160	1,120	2,160	2,800	2,880	3,600	3,600	3,360	1,680	2,520
	PCIe® Gen2[2]		3	4	—	—	4	—	—	—	—	—	—
	PCIe Gen3		—	—	2	2	—	2	3	3	4	2	3
	Analog Mixed Signal (AMS) / XADC		1	1	1	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks		1	1	1	1	1	1	1	1	1	1	1
	GTX Transceivers (12.5 Gb/s Max Rate)[3]		36	36	—	—	56	—	—	—	—	—	—
	GTH Transceivers (13.1 Gb/s Max Rate)[4]		—	—	28	48	—	80	80	72	96	48	72
	GTZ Transceivers (28.05 Gb/s Max Rate)		—	—	—	—	—	—	—	—	—	8	16
Speed Grades	Commercial		-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended[5]		-2L, -3	-2L, -2G	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L	-2L, -2G	-2L, -2G	-2L, -2G
	Industrial		-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1	—	—
	Package[6]	Dimensions (mm)	**Available User I/O:** 3.3V HR I/O, 1.8V HP I/Os (GTX, GTH)									1.8V HP I/O (GTH, GTZ)	
	FFG1157 / FFV1157[7]	35 x 35	0, 600 (20, 0)		0, 600 (0, 20)	0, 600 (0, 20)	0, 600 (20, 0)		0, 600 (0, 20)				
Footprint Compatible	FFG1761 / FFV1761[7]	42.5 x 42.5	100, 750 (36, 0)		50, 650 (0, 28)		0, 700 (28, 0)		0, 850 (0, 36)				
	FHG1761	45 x 45		0, 850 (36, 0)									
	FLG1925	45 x 45		0, 1200 (16, 0)									
	FFG1158 / FFV1158[7]	35 x 35				0, 350 (0, 48)	0, 350 (48, 0)	0, 350 (0, 48)	0, 350 (0, 48)				
Footprint Compatible	FFG1926	45 x 45							0, 720 (0, 64)	0, 720 (0, 64)			
	FLG1926	45 x 45									0, 720 (0, 64)		
	FFG1927 / FFV1927[7]	45 x 45				0, 600 (0, 48)	0, 600 (56, 0)	0, 600 (0, 80)	0, 600 (0, 80)				
Footprint Compatible	FFG1928	45 x 45								0, 480 (0, 72)			
	FLG1928	45 x 45									0, 480 (0, 96)		
Footprint Compatible	FFG1930	45 x 45					0, 700 (24, 0)		0, 1000 (0, 24)	0, 900 (0, 24)			
	FLG1930	45 x 45									0, 1100 (0, 24)		
	FLG1155	35 x 35										400 (24, 8)	
	FLG1931	45 x 45										600 (48, 8)	
	FLG1932	45 x 45											300 (72, 16)

XMP084 (v4.11)

FFG/FFV/FLG/FHG: 1.0 mm Flip-chip fine-pitch BGA

Notes: 1. EasyPath™ solutions provide a fast and conversion-free path for cost reduction.
2. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
3. 12.5 Gb/s support in "-3E", "-2GE" speed/temperature grade; 10.3125 Gb/s support in "2C", "-2LE", and "-2I" speed grade.
4. 13.1 Gb/s support in "-3E". "-2GE" speed grade; 11.3 Gb/s support in "2C" , "-2LE" and "-2I" speed/temperature grades.
5. -2G only applies to Stacked Silicon Interconnect devices and supports 12.5G GTX, 13.1G GTH, 28.05G GTZ with -2 fabric.
6. Leaded package options ("FFxxxx"/"FLxxxx"/"FHxxxx") available for all packages. "HCxxxx" is not offered in a leaded option.
7. FFV packages are only available in XC7VX330T and XC7VX415T devices. See DS180, *7 Series FPGAs Overview* for package details.