XA Artix®-7 FPGAs

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			XA Artix®-7 FPGAs Optimized for Lowest Cost and Lowest Power Applications (1.0V)				
	Part Number		XA7A15T	XA7A35T	XA7A50T	XA7A75T	XA7A100T
Logic Resources	Logic Cells		16,640	33,280	52,160	75,520	101,440
	Slices		2,600	5,200	8,150	11,800	15,850
	CLB Flip-Flops		20,800	41,600	65,200	94,400	126,800
Memory Resources	Maximum Distributed RAM (Kb)		200	400	600	892	1,188
	Block RAM/FIFO w/ ECC (36 Kb each)		25	50	75	105	135
	Total Block RAM (Kb)		900	1,800	2,700	3,780	4,860
Clock Resources	CMTs (1 MMCM + 1 PLL)		5	5	5	6	6
I/O Resources	Maximum Single-Ended I/O		210	210	210	285	285
	Maximum Differential I/O Pairs		100	100	100	137	137
Integrated IP Resources	DSP Slices		45	90	120	180	240
	PCIe® Gen2[1]		1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC		1	1	1	1	1
	Configuration AES / HMAC Blocks		1	1	1	1	1
	GTP Transceivers (6.25 Gb/s Max Rate)[2]		4	4	4	4	4
Speed Grades	Industrial (–40°C to +100°C)		-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Automotive (–40ºC to +125ºC)		-1	-1	-1	-1	-1
	Package	Dimensions (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O (GTP Transceivers)				
	CPG236	10 x 10	100 (2)	100 (2)	100 (2)		
	CSG324	15 x 15	210 (0)	210 (0)	210 (0)	210 (0)	210 (0)
	CSG325	15 x 15	150 (4)	150 (4)	150 (4)		
	FGG484	23 x 23				285 (4)	285 (4)

XMP095 (v1.1)

CPG: 0.5mm Wire-bond chip-scale; **CSG**: 0.8mm Wire-bond chip-scale; **FGG**: 1.0mm Wire-bond fine-pitch

Notes: 1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. GTP transceiver: 6.25 Gb/s available in -2 speed grade only; 3.75 Gb/s in -1 speed grade.