

AcceIDSP Synthesis Tool

Release Notes

Release 10.1.1 April, 2008





Xilinx is disclosing this Document and Intellectual Property (hereinafter "the Design") to you for use in the development of designs to operate on, or interface with Xilinx FPGAs. Except as stated herein, none of the Design may be copied, reproduced, distributed, republished, downloaded, displayed, posted, or transmitted in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx. Any unauthorized use of the Design may violate copyright laws, trademark laws, the laws of privacy and publicity, and communications regulations and statutes.

Xilinx does not assume any liability arising out of the application or use of the Design; nor does Xilinx convey any license under its patents, copyrights, or any rights of others. You are responsible for obtaining any rights you may require for your use or implementation of the Design. Xilinx reserves the right to make changes, at any time, to the Design as deemed desirable in the sole discretion of Xilinx. Xilinx assumes no obligation to correct any errors contained herein or to advise you of any correction if such be made. Xilinx will not assume any liability for the accuracy or correctness of any engineering or technical support or assistance provided to you in connection with the Design.

THE DESIGN IS PROVIDED "AS IS" WITH ALL FAULTS, AND THE ENTIRE RISK AS TO ITS FUNCTION AND IMPLEMENTATION IS WITH YOU. YOU ACKNOWLEDGE AND AGREE THAT YOU HAVE NOT RELIED ON ANY ORAL OR WRITTEN INFORMATION OR ADVICE, WHETHER GIVEN BY XILINX, OR ITS AGENTS OR EMPLOYEES. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE DESIGN, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND NONINFRINGEMENT OF THIRD-PARTY RIGHTS.

IN NO EVENT WILL XILINX BE LIABLE FOR ANY CONSEQUENTIAL, INDIRECT, EXEMPLARY, SPECIAL, OR INCIDENTAL DAMAGES, INCLUDING ANY LOST DATA AND LOST PROFITS, ARISING FROM OR RELATING TO YOUR USE OF THE DESIGN, EVEN IF YOU HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. THE TOTAL CUMULATIVE LIABILITY OF XILINX IN CONNECTION WITH YOUR USE OF THE DESIGN, WHETHER IN CONTRACT OR TORT OR OTHERWISE, WILL IN NO EVENT EXCEED THE AMOUNT OF FEES PAID BY YOU TO XILINX HEREUNDER FOR USE OF THE DESIGN. YOU ACKNOWLEDGE THAT THE FEES, IF ANY, REFLECT THE ALLOCATION OF RISK SET FORTH IN THIS AGREEMENT AND THAT XILINX WOULD NOT MAKE AVAILABLE THE DESIGN TO YOU WITHOUT THESE LIMITATIONS OF LIABILITY.

The Design is not designed or intended for use in the development of on-line control equipment in hazardous environments requiring fail-safe controls, such as in the operation of nuclear facilities, aircraft navigation or communications systems, air traffic control, life support, or weapons systems ("High-Risk Applications"). Xilinx specifically disclaims any express or implied warranties of fitness for such High-Risk Applications. You represent that use of the Design in such High-Risk Applications is fully at your risk.

© 2002-2008 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo, and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

Table of Contents

Chapter 1: Release 10.1.1

Tools and Flow Integration.....	5
---------------------------------	---

Chapter 1: Release 10.1

AccelDSP Enhancements	7
Native Complex Number Support	7
More Efficient Mapping to BlockRAMs	7
Tools and Flow Integration.....	7

Chapter 1: Release 9.2.01

AccelDSP Enhancements	9
I/O Port Width Limit Expanded to 53 Bits	9
Simulation Vectors Displayed As Decimal Values	9
New Project Option Limits the Maximum Fractional Length for Input Ports	10
Spartan-3A DSP 1800A Starter Platform Now Supported	10
Spartan-3A DSP 3400A Development Platform Now Supported	10
Tools and Flow Integration.....	10

Chapter 2: Release 9.2.00

AccelDSP Enhancements	11
Ease of Use and Tools/Flow Integration	11
Quality of Results.....	12
Tools and Flow Integration.....	13

Release 10.1.1

Tools and Flow Integration

AccelDSP Synthesis is currently compatible with the following tools:

Table 1-1: AccelDSP Compatibility with Other Tools

Tool	Version
The Mathworks MATLAB®, Simulink Fixed-Point Toolbox	2007a and 2007b
Mentor Graphics ModelSim® SE	6.3c
Mentor Graphics Precision™ RTL Synthesis	2006a.101
Microsoft® Internet Explorer	6.0 or later
Synplicity Synplify Pro®	8.8.0.4 (requires a floating license from Synplicity for AccelDSP integrated optimization)
Xilinx® ISE	10.1.1
Xilinx® ISE Simulator	10.1.1
Xilinx® System Generator	10.1.1

Release 10.1

AccelDSP Enhancements

Native Complex Number Support

AccelDSP can now synthesize MATLAB written using built-in complex numbers. For example, the following code can now be synthesized into RTL:

```
function y = my_design(x)
A = 3+4i;
y = (x + A) * -3i / 2;
```

Refer to the manual *MATLAB for Synthesis Style Guide* on supported functions.

More Efficient Mapping to BlockRAMs

Previously, AccelDSP could schedule a BlockRAM to be written to and read from in a single cycle. Now two values can be read from or written to a BlockRAM in a single cycle. This doubles the throughput attainable from each BlockRAM.

Tools and Flow Integration

AccelDSP Synthesis is currently compatible with the following tools:

Table 1-1: AccelDSP Compatibility with Other Tools

Tool	Version
The Mathworks MATLAB®, Simulink Fixed-Point Toolbox	2007a and 2007b
Mentor Graphics ModelSim® SE	6.3c
Mentor Graphics Precision™ RTL Synthesis	2006a.101
Microsoft® Internet Explorer	6.0 or later
Synplicity Synplify Pro®	8.8.0.4 (requires a floating license from Synplicity for AccelDSP integrated optimization)
Xilinx® ISE	10.1
Xilinx® ISE Simulator	10.1
Xilinx® System Generator	10.1

Release 9.2.01

AccelDSP Enhancements

I/O Port Width Limit Expanded to 53 Bits

AccelDSP now supports input and output quantization up to 53 bits for unsigned numbers and 54 bits for signed numbers. The previous limit was 31 bits for unsigned numbers and 32 bits for signed numbers. To enable this feature, the test vectors are now stored on disk in hexadecimal format instead of integer format.

– Fixed Point Information: **iir_filter** 1 maximum quantization

– Inputs

Name	Shape	Quantizer	Quantizer Source
sample	1 x 1	fixed floor wrap [48 36]	Directive (delete)

– Outputs 1 maximum quantization

Name	Shape	Quantizer	Quantizer Source
y	1 x 1	fixed floor wrap [54 40]	Directive (delete) - maximum

Simulation Vectors Displayed As Decimal Values

AccelDSP now displays fixed-point simulation vectors in decimal format. Previously they were displayed as integers with the binary point removed. This new format allows for easier interpretation of the fixed-point vectors.

Time (ns)	# of Clocks Since Last Output	Fixed Point Simulation Values	RTL Simulation Values
0	reset		
450	1	2.217712402343750e-001	2.217712402343750e-001
550	1	1.476226806640625e+000	1.476226806640625e+000
650	1	3.536071777343750e-001	3.536071777343750e-001

New Project Option Limits the Maximum Fractional Length for Input Ports

To help prevent unnecessary precision on AccelDSP inputs, a new project option has been added that limits the maximum fractional length for input ports. The range is 1-53 bits. The default is 12 bits. The quantization of any input can be changed with a directive on that input. You can also change the maximum fractional length from the Project Options dialog box or you can enter a command line from the Tcl Console similar to the following:

```
SetProjectOption -quantizer_max_input_fractional_length 10
```

Spartan-3A DSP 1800A Starter Platform Now Supported

AccelDSP now supports the Spartan-3A DSP 1800A Starter Platform for Ethernet Point-to-Point Hardware Co-Simulation.

Spartan-3A DSP 3400A Development Platform Now Supported

AccelDSP now supports the Spartan-3A DSP 3400A Development Platform for Hardware Co-Simulation. Both the Point-to-point Ethernet configuration as well as the Network-Based Ethernet configuration are supported.

Tools and Flow Integration

AccelDSP Synthesis is currently compatible with the following tools:

Table 1-1: AccelDSP Compatibility with Other Tools

Tool	Version
The Mathworks MATLAB®, Simulink Fixed-Point Toolbox	2006b and 2007a
Cadence® NC-Sim	5.4 SO-20
Mentor Graphics ModelSim® SE	6.1f
Mentor Graphics Precision™ RTL Synthesis	2006a.101
Mentor Graphics Leonardo Spectrum™	2005a.76
Microsoft® Internet Explorer	6.0 or later
Synplicity Synplify Pro®	8.8.0.4 (requires a floating license from Synplicity for AccelDSP integrated optimization)
Xilinx® ISE	9.2.03i
Xilinx® ISE Simulator	9.2.03i
Xilinx® System Generator	9.2.01

Release 9.2.00

AccelDSP Enhancements

Ease of Use and Tools/Flow Integration

Single DSP Tools Installer

Now both System Generator and AccelDSP are available via a single download and installer. System Generator also has additional flexibility in where it can be installed. The software is enabled via a Xilinx registration ID. AccelDSP no longer requires a FlexLM license. The AccelWare Advanced Math Toolkit and Communications Toolkit IP libraries still require a FlexLM license.

System Generator MATLAB Selector

During the unified installation process, this configuration feature allows the user additional flexibility to specify which version of MATLAB/Simulink should be associated with a particular version of System Generator. This is helpful for users who have more than one version of MATLAB/Simulink or System Generator on their machine.

Improved AccelDSP to System Generator Flow

The generation of System Generator blocks from AccelDSP has been enhanced to improve ease-of-use. With this enhancement, rate changes are automatically accounted for by System Generator and more optimized hardware for multi-rate designs will now be generated. An additional benefit includes being able to place multiple instances of a single AccelDSP generated block in a System Generator design.

Clock Enable Support Added

AccelDSP now can optionally generate an interface including a clock enable input port. This adds flexibility when connecting an AccelDSP generated block into larger systems. The feature is controlled by a project option.

Selectable Block Frequency for Hardware Co-Simulation

When you are using hardware co-simulation with a Xilinx ML402 or ML506 platform, AccelDSP allows you to choose a clock frequency for the target design that is equal to or less than the system clock frequency. The following table outlines the frequencies that are available:

Platform	Interface	System Clock Frequency	Available Frequencies (Ratios)
Xilinx ML402	JTAG, Point-to-point Ethernet, Network-based Ethernet	100 MHz	100 MHz 66.7 MHz 50 MHz 33.3 MHz
Xilinx ML506	Point-to-point Ethernet, Network-based Ethernet	200 MHz	100 MHz 66.7 MHz 50 MHz 33.3 MHz

Quality of Results

Improved Fmax on Designs with Large CE Fanout

For designs that are created with the System Generator Synthesis Flow, this improvement is made possible through new features in System Generator and the ISE Mapper. See the System Generator documentation for information on how to setup the CE fanout reduction options.

Tools and Flow Integration

AccelDSP Synthesis is currently compatible with the following tools:

Table 2-1: AccelDSP Compatibility with Other Tools

Tool	Version
The Mathworks MATLAB®, Simulink Fixed-Point Toolbox	2006b and 2007a
Cadence® NC-Sim	5.4 SO-20
Mentor Graphics ModelSim® SE	6.1f
Mentor Graphics Precision™ RTL Synthesis	2006a.101
Mentor Graphics Leonardo Spectrum™	2005a.76
Microsoft® Internet Explorer	6.0 or later
Synplicity Synplify Pro®	8.8.0.4 (requires a floating license from Synplicity for AccelDSP integrated optimization)
Xilinx® ISE	9.2.02i
Xilinx® ISE Simulator	9.2.02i
Xilinx® System Generator	9.2.00

