# PlanAhead Release Notes

*What's New in the 11.2 Release*

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# What's New in the PlanAhead 11.2 Release

This document provides an overview of the new features and functionality included in the PlanAhead™ 11.2 release over those available in the 11.1 release. Beginning with the ISE® 11 release, Xilinx has replaced the service pack release naming convention with numbered incremental releases (11.2 versus 11.1 SP2). This was done to better reflect our commitment to delivering not just bug fixes, but also feature enhancements that are deemed important enough not to wait for a yearly major release. For details on the functionality in the 11.1 release, please refer to the PlanAhead and ISE 11.1 documentation and release notes.

This document assumes that users will upgrade to ISE11.2 at some point. However, users electing to use previous ISE versions will still see significant benefits in migrating to PlanAhead 11.2. Support is available for versions of ISE 6.1i and later.

For more information, please refer to the *PlanAhead User Guide* or contact the Xilinx Technical Support. For contact information, visit www.xilinx.com/support

## Device Support

PlanAhead 11.2 introduces device support for Virtex®-6 and Spartan®-6 devices. In addition, PlanAhead 11.2 fully supports all of the available Virtex-4, Virtex-5 and Spartan-3 FPGA devices. Virtex, Virtex-II, Virtex-II Pro and Spartan 2 device family support has been removed from ISE 11.1 software. ISE software version 10.1 or earlier should be used to design with those devices.

As new devices are introduced, they will be made available in PlanAhead through minor update releases. It is advisable to remain current with the PlanAhead update releases using the Xilinx Update capabilities. Update releases are distinguished by the last digit in the release number (11.2, 11.3, etc.).

PlanAhead 11.2 offers support for the following device families:

| | |
|---|---|
| Virtex-6 LX | Spartan-6 |
| Virtex-6 LXT | Spartan-3A DSP |
| Virtex-6 CXT | Spartan-3AN |
| Virtex-6 SXT | Spartan-3A |
| Virtex-6 Lower Power | Spartan-3E |
| Virtex-5 TXT | Spartan-3 |
| Virtex-5 FXT | Virtex-4 SX |
| Virtex-5 SXT | Virtex-4 LX |
| Virtex-5 LXT | Virtex-4 FX |
| Virtex-5 LX | |
| Virtex-5 QPro | |

# Installation and Licensing

All of the Xilinx® software tools migrated to FlexNet-based licensing with the 11.1 release. Please refer to the *ISE Design Suite 11: Installation, Licensing, and Release Notes* for more information about installing the software, obtaining licenses and configuring the license manager.

### Incremental Releases

Incremental PlanAhead Update releases will be made available using the existing *Xilinx Update* mechanism. Running *Xilinx_Update* will alert users of new PlanAhead releases and prompt to download and install the updates.

## New PlanAhead Features

# Device Support

PlanAhead 11.2 introduces support for Virtex-6 and Spartan-6 devices. These are two new device families that are in the first public access release phase, and are not yet in full production. PlanAhead supports the following basic features for these new devices:

- Device Exploration – view physical resources for devices
- I/O Pin Planning - Drag and drop of ports for assignment
- Floorplanning
- Design Analysis
  - Import placement results from routed ncd
  - Import timing results from TRCE path reports
- TimeAhead – basic support, production speed files are not yet available for these devices
- DRC – device-specific design rule checks
- Synthesis and Implementation Runs
- Project Navigator Integration

# I/O Pin Planning

PlanAhead 11.2 includes several enhancements to the PinAhead environment, as described below.

### Alternate Compatible Devices

For Virtex-6, PlanAhead now includes the ability to define alternate compatible parts to support different devices with compatible packages. This feature is not available in any of the Spartan-6 devices at this time.

### New DRCs

Many new device-related DRCs have been added to PlanAhead 11.2. Please review Chapter 5, "I/O Pin Planning" of the *PlanAhead User Guide* for information about the various I/O DRCs.

### New Constraint Support

PlanAhead supports new IN_TERM and OUT_TERM constraints for Spartan-6 devices.

# GUI

PlanAhead 11.2 includes many enhancements to the GUI, including:

1. There have been significant speedup and memory improvements in the GUI when drawing fully-placed designs.
2. Site names are now drawn in the device view within the GUI.
3. The view search field now filters selections as well as displayed items.
4. Multiple source file adding and disabling files has been made much faster.
5. Selecting many primitives is much faster
6. Improved support for Japanese language installs.
7. Improved support for Verilog source file editing.
8. View filtering works for trees as well as tables.
9. PlanAhead now allows copy and paste of elaboration messages
10. Removal of default shortcuts is now allowed.
11. Improved startup performance on 64-bit Linux.

# Miscellaneous

1. PlanAhead now imports part information from ngc files. *Ngc2edif* now exports the part information in the generated EDIF, and PlanAhead will parse it and use it as the default part for the project. We will also issue warnings if instantiated ngc cores reference a part that is different than the part assigned to the top-level netlist.
2. In Project Navigator integration mode, PlanAhead now echoes warning messages to the console window and log file for constraints that are not understood. Previously these constraints were passed silently through PlanAhead and preserved in the Project Navigator source UCF, but no warnings were generated to give the user the opportunity to correct any problems in the UCF.

# Known Issues

### Automatic placement of pblocks is not enabled for Spartan-6 devices.

Automatic placement and sizing of pblocks is not supported yet in this new device family.

Solution:

Users can still manually draw rectangles, place, and resize pblocks in the GUI.