Pin Planning Methodology Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/2011	13.1	Initial version

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Pin Planning Methodology

The *Pin Planning Methodology Guide* recommends an Input/Output (I/O) pin planning methodology for Xilinx® devices using the PlanAhead™ software.

The PlanAhead software and its I/O planning environment:

- Provide a design flow from Register Transfer Level (RTL) to bit stream.
- Allow you to:
  - Create, import, and configure the initial list of I/O ports early in the design flow.
  - Perform final verification of the pinout at the end of the design flow.
  - Group related ports into interfaces, then assign them to package pins.
  - Use fully automatic pin placement or semi-automated interactive modes for controlled I/O port assignment.
  - View the relationship of the physical package pins and banks with their corresponding I/O die pads.
  - Make intelligent decisions to optimize the connectivity between the PCB and the FGPA device.

The I/O pin planning methodology recommended by Xilinx includes the steps shown in the following section, Pin Planning Methodology Steps.

Pin Planning Methodology Steps

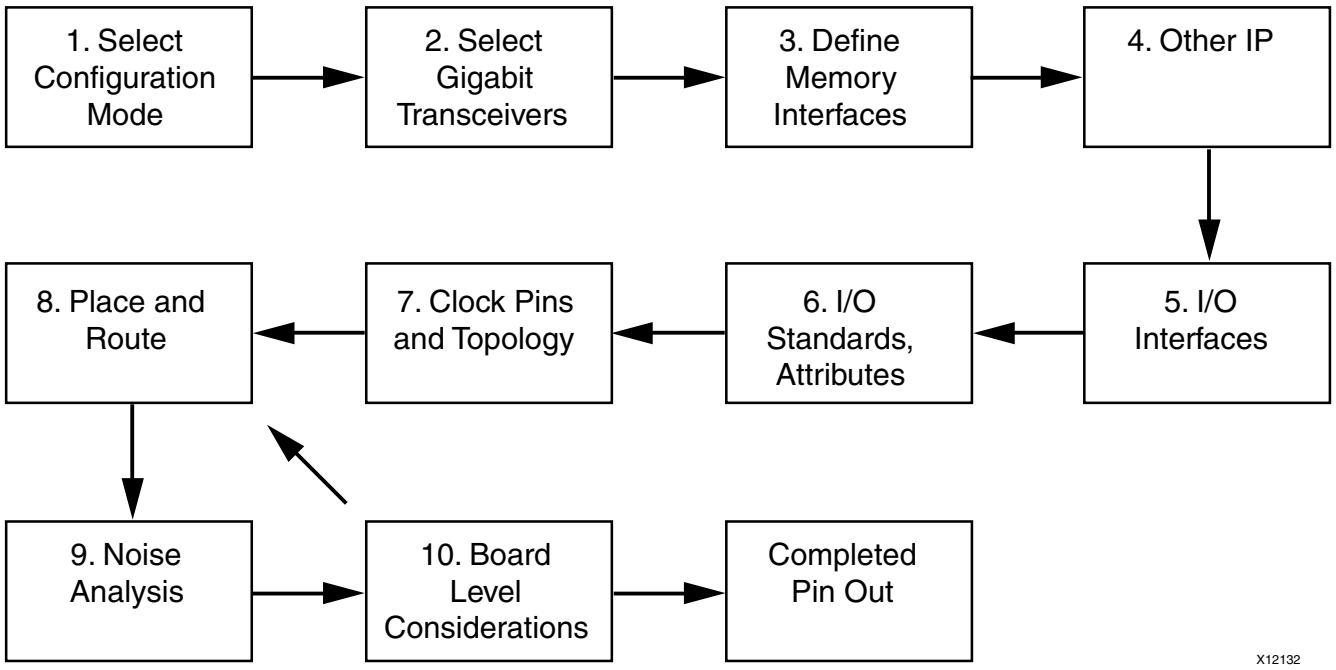

Figure 1-1: Xilinx Recommended Pin Planning Methodology

1. Select Configuration Mode

- Most configuration modes share some pins with User I/O. The number of shared pins typically:
  - Is *none* to *small* for serial modes.
  - Grows larger for parallel modes.
- Avoid signal contention to ensure successful configuration. If I/Os are used after configuration, they must be changed to tri-state during configuration.
- If the design allows, prohibit all dual-purpose pins to simplify the pinout.
- For more information, see the *Configuration User Guide* for each device family referred to in Additional Resources. The guides describe the dedicated and shared configuration pins for each mode. Check the user guide to see if certain configuration modes create additional pinout restrictions.

2. Select Gigabit Transceivers

- Gigabit transceivers (GTs):
  - Have a set of dedicated pins.
  - Typically share clock pins with other GTs or I/O clock regions.
- Adjacent to the GTs, most device families list which user I/Os to avoid in order to achieve optimal signal integrity.
- For more information, see the *Gigabit Transceivers User Guide* for each device family referred to in Additional Resources.

3. Define Memory Interfaces

- High speed memory interfaces have specific pinout requirements driven by clocking and skew needs.
- The Memory Interface Generator (MIG) software generates the required pinouts.

4. Other IP

- Some Intellectual Property (IP) such as the PCIe® software has specific pinout requirements.
- Use the CORE Generator™ software to incorporate any IP with external interfaces into the design.
- Like the Memory Interface Generator (MIG) software, the Xilinx CORE Generator software generates the required pinout constraints.

5. I/O Interfaces

- Define any additional I/O interfaces.

6. I/O Standards, Attributes

- Define the I/O standards and other attributes.
- Run a Design Rules Check (DRC) in the PlanAhead software to check I/O standard versus I/O banking restrictions.
- Some I/O standards can be combined within a single bank and some cannot. For information on the packaging and pinout specifications for specific device families, see the Packaging and Pinout guides available from the Xilinx support website. See, for example, the *Virtex-6 FPGA Packaging and Pinout Specifications (UG365)* referred to in Additional Resources.

7. Clock Pins and Topology

- Use the dedicated external clock pins on the FPGA device for best clock performance.
- Understand the following:
  - I/O versus fabric clocking resources.
  - Regional clock restrictions in the device family.
- Designs with fewer clocks than the number of global clock resources are usually simpler.
- For more complex clock structures, enter the clock tree and enough loads to run the early design through place and route for validation.
- Complex clock structures include designs with high clock counts that require either automatic or manual floor planning to utilize regional clocks
- To aid in clock planning, the PlanAhead software displays a graphical representation of the available clock resources for the target device.
- For more information on Clock Resources View, see the *Clocking Resources User Guide* for each device family referred to in Additional Resources.

8. Place and Route

- By this point, most if not all of the primary structures (I/O, IP, and Clocking) should be defined. The more primary structures that are defined and available, the more accurate are the associated DRCs.
- Run the design through place and route to validate the pinout.
- Not all logic needs to be in place, only the primary structures that affect pinout.
- Fully implement the design in order to ensure a legal I/O pinout.
- Review the **`ngdbuild`** and **`map`** reports for I/O and clock-related messages.
- Only the place and route tools contain all sign-off DRCs on the final design and pinout.

9. Noise Analysis

Table 1-1: **Noise Analysis Methods Supported in the PlanAhead Software**

Method	Supported Devices
Simultaneous Switching Noise (SSN)	• Spartan®-6 • Virtex®-6
Weighted Average Simultaneous Switching Output (WASSO)	• Spartan-3 • Virtex-4 • Virtex-5

- To improve results when a violation occurs:
  - Use I/O standards that have a lower noise impact for the failing group.
  - Reduce noise by changing to a:
    - Lower drive strength.
    - Parallel-terminated DCI I/O standard.
    - Lower class of driver.

    Example: Changing the SSTL Class II to an SSTL Class I.
  - Relocate the pin within the bank to an alternate location that is a greater distance from other noisy pins.
  - Spread the failing pins across multiple banks. This reduces the number of aggressive outputs on the power system of one bank.
  - Spread the failing group across multiple synchronous phases.
- If the design changes:
  - Rerun 8. Place and Route.
  - Return to 9. Noise Analysis.
- For more information, see the *PlanAhead User Guide (UG632)* referred to in Additional Resources.

10. Board Level Considerations

- For board-level validation, perform signal integrity analysis using IBIS (Input/Output Buffer Information Specification) or HSPICE models.
- To optimize the pinout within the context of the entire board, import the FPGA pinout into third party products such as:
  - *Cadence Allegro FPGA System Planner*
  - Mentor Graphics I/O Designer
- If the pinout changes:
  - Rerun 8. Place and Route.
  - Continue from that step on.

Additional Resources

- For definitions of terms, see the Xilinx Global Glossary at: http://www.xilinx.com/support/documentation/sw_manuals/glossary.pdf
- Find other Xilinx Documentation at: http://www.xilinx.com/support/documentation
- To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see Xilinx Support at: http://www.xilinx.com/support
- For information on I/O pin planning and flows in the PlanAhead software, see the *PlanAhead Software Tutorial - I/O Pin Planning (UG674)* at: http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/PlanAhead_Tutorial_IO_Pin_Planning.pdf
- For information on the packaging and pinout specifications for specific device families, see the Packaging and Pinout guides available from the Xilinx support website at http://www.xilinx.com/support/documentation. See, for example, the *Virtex-6 FPGA Packaging and Pinout Specifications (UG365)* at: http://www.xilinx.com/support/documentation/user_guides/ug365.pdf
- For information on PlanAhead functionality and commands, see "I/O Pin Planning" in the *PlanAhead User Guide (UG632)* at: http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/PlanAhead_UserGuide.pdf
- For information on configuration mode, see the *Configuration User Guide* for each device family available from the Xilinx support website at: http://www.xilinx.com/support/documentation
- For information about Gigabit Transceivers, see the *Gigabit Transceivers User Guide* for each device family available from the Xilinx support website at: http://www.xilinx.com/support/documentation
- For more information on Clock Resources View, see the *Clocking Resources User Guide* for each device family available available from the Xilinx support website at: http://www.xilinx.com/support/documentation

- For information on the following third party pin planning tools that support Xilinx FPGA pin planning at the board level, see:
  - *Cadence Allegro FPGA System Planner (FSP)* at:

    www.cadence.com
  - *Mentor Graphics I/O Designer* at:

    www.mentor.com