

Xilinx Design Tools: Release Notes Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/08/2012	14.1	Initial Xilinx release.

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What's New in Xilinx Design Tools

Vivado Design Suite 2012.1 Release

Vivado™ Design Suite, Xilinx's new IP and system-centric design environment, has been released for Early Access to select customers. Release notes for Vivado Design Suite 2012.1 are only available to Early Access customers. For more information on Vivado Design Suite, see <http://www.xilinx.com/products/design-tools/vivado/index.htm>

ISE Design Suite 14.1

Device Support

- Public access is now available for the following families:
 - Zynq™-7000 EPP (including bitstream generation)
 - Defense-grade 7 series FPGA and Zynq-7000 EPP
 - Automotive XA Zynq-7000 EPP
- Virtex®-7 XT FPGA family now supports bitstream generation.
- Artix™-7 FPGA GTPE2 support is now available, which includes:
 - SecureIP simulation models for all Xilinx-supported simulators.
 - 7 series FPGA GT Transceiver Wizard support.
- The following Artix-7 devices have been removed from the tools:
 - XC7A8
 - XC7A15
 - XC7A30T
 - XC7A50T

- ISE® Design Suite requires users to select all IO Standards and pin-placement in their designs prior to generating a bitstream. Please see the following Xilinx Answer Record for more information: <http://www.xilinx.com/support/answers/41615.htm>

PlanAhead Design Tool

More information on new features described in this chapter can be found in the *PlanAhead™ Design Tool User Guide*:

www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/PlanAhead_UserGuide.pdf

General

- The Flow Navigator now provides a more detailed view of the steps involved in the compilation flow. This includes the ability to easily collapse and expand the list of detailed tasks available within each design view (RTL Analysis, Synthesis, Implementation, and Program and Debug).
- The new clock resource view now displays connectivity of clocking and IO related resources using fly lines.
- Project settings now include more XPA options.

Pin Planning

- The PlanAhead design tool now provides the ability to convert pin-planning projects from an empty netlist project to a full RTL or netlist-based project. This allows you to migrate pin planning projects to more useful projects that manage more source types.
- Pin-planning support for Zynq-7000 EPP devices is now available.
- Pin-planning projects can now automatically infer differential pairs by recognizing one side of a differential standard and by providing the ability to automatically create the other side of the differential pair.
- There is an improved Simultaneous Switching Noise (SSN) reporting engine and improved 7 series FPGA noise prediction.
- There are improvements on the presentation of default IO standards.

Modelsim & Questa Advanced Simulator Integration

- The PlanAhead design tool now allows you to choose Modelsim or Questa® Advanced Simulator as the target simulator in the project settings. Simulation requires library compilation, which can be accomplished through Tcl command `compplib`. The main advantage of this integration over ISE tools integration is the ability to have multiple simulation filesets with their own sets of properties. This allows you to simultaneously create and maintain multiple simulation configurations that could vary depending on the testbench being used or other simulation properties.

Embedded Development Kit Integration

- The PlanAhead design tool can now create and add Xilinx Platform Studio (XPS) subsystems to a project through the `.xmp` source type. Double-clicking the `.xmp` source type launches Xilinx Platform Studio to generate and customize the embedded subsystem.
- Integration support also includes importing and converting ISE tools projects (`.xise`) that have `.xmp` sources embedded within them to PlanAhead design tool projects. The PlanAhead design tool manages generated files from XPS appropriately in the synthesis and implementation tool flows.

System Generator for DSP Integration

- PlanAhead design tool can now create and add DSP subsystems to a project through the `.sgp` source type. Double clicking the `.sgp` source type launches The MathWorks Simulink® to generate and customize the DSP subsystem.
- Integration support includes importing and converting ISE tools projects (`.xise`) that have `.sgp` sources embedded within them to PlanAhead design tool projects. PlanAhead design tool manages generated files from the DSP tools appropriately in the synthesis and implementation tool flows.

IP Repository

- PlanAhead design tool now allows the use of the IP repository without creating a design. You can create an empty project and open the IP repository for browsing, generating, and configuring an IP core. Generated sources, such as example designs, constraint files, data sheets, and more are now viewable in the project with a special IP Sources tab in the sources view.
- Initial support for the IEEE P1735 encryption standards.

Runs Infrastructure

- PlanAhead design tool can now force a run up-to-date if it has been marked stale and the user wishes to override the tool.
- Physical constraint updates do not cause the synthesis run state to go stale.
- There is a new "next step" option to run to intermediate states of the ISE tools (e.g. `ngdbuild`, `map`, `par`, `trce`).
- Bitgen options are now integrated with run options in project settings.
- There is now support for optional steps in the flow, as well as a mechanism to invoke Tcl "hook" scripts for use between stages of the run flow. You can specify a Tcl script that runs between compilation stages, you can use it for custom workarounds or reporting purposes.

Project Infrastructure

- Messages are now centralized to a common message manager, and should be visible in the messages tabs.
- PlanAhead design tool can now reset parameters and properties with the new Tcl commands `reset_param` and `reset_property`. These commands reset the value of the property and parameter to the built-in default, and if appropriate, to the specific target device.
- Certain invalid UCF messages are disabled for RTL elaboration
- Improved falsely reported error and critical warning conditions when parsing UCF on RTL netlists.
- Improved include file support in RTL.

Embedded Design Tools

Embedded Design improvements in 14.1 are focused on 4 main areas:

- Zynq-7000 EPP support for bare-metal and Linux-based product development
- MicroBlaze™ processor updates
 - Performance improvements
 - New instructions for endianness conversion
 - Pre-integrated IO module
 - Multi-processor lock-step/result-voting for tamper & single event upset detection
 - Additional device support
- IP updates for improved system performance, configuration, and utility
- Tools updates for XPS and SDK

Zynq-7000 EPP Support

- 14.1 ISE WebPACK™ design tools now support Zynq-7000 EPP for the Xilinx Z7010, Z7020, Z7030 parts. Included in WebPACK design tools are the same tools as the Embedded Edition – XPS, SDK, MicroBlaze processor, and the full embedded IP library.
- XPS includes new configuration and MIO summary windows dedicated to Zynq-7000 EPP (see Embedded Tools below for further information).
- Zynq-7000 EPP documents are now available on the Xilinx website and also via the Xilinx Documentation Navigator tool which can be downloaded from <http://www.xilinx.com/support>.

MicroBlaze Processor Updates

New Low-latency interrupt mode

- The controller directly supplies the interrupt vector resulting in a reduction in latency response by as much as 10X depending on system design.

New Swap instructions

- New instructions for byte and halfword swapping help support endianness conversions between AXI big-endian and AXI little-endian.

Additional Device Support

- MicroBlaze processor has been validated across Xilinx 7 series FPGA families.

System Cache

- Embedded Edition adds a new embedded system cache IP peripheral between a MicroBlaze processor and external memory controller for AXI-based systems. MicroBlaze processor uses this System Cache IP core as Level 2 cache resulting in lower latency and faster performance depending on multiple system factors, design type, or connection points.

IO Module

- A new, configurable collection of general embedded processor peripherals packaged into a single IP block for connection to the MicroBlaze processor data-side LMB bus. This simplifies the definition, configuration and deployment of a standard Microcontroller system and enables MicroBlaze processor MCS designs to be moved seamlessly from Logic Edition into Embedded Edition.

Embedded IP Updates

14.1 includes IP core enhancements and additions focus on improved support for AXI, Zynq-7000 EPP, and MicroBlaze processor.

- AXI Quad SPI - Supports Execute In Place (XIP) mode and architectural improvements for performance. This IP core continues to work in Legacy mode as default option for existing customer.
- AXI Performance Monitor - Measures bus latency of a specific master/slave (AXI4/AXI4-Lite/AXI4-Stream) in a system, the amount of memory traffic for specific durations, and other performance metrics.
- Processing System7 - Wrapper IP for Zynq-7000 EPP, logic connection between PS and PL to assist with adding custom or other EDK IP.

- AXI System Cache - Level 2 Cache module for MicroBlaze processor when used in between MicroBlaze processor and external memory controller.
- Embedded IO Module - Common IO peripheral sub-set, introduced in MicroBlaze processor MCS, ported to Embedded Edition for compatibility.

Embedded Tools

In ISE Design Suite 14.1, the PlanAhead design tool now supports embedded design capture and management and is the recommended embedded design flow.

What's New in XPS?

In 14.1, XPS has been extended to provide Zynq-7000 EPP specific tools for configuration and first-stage bootloader generation with SDK.

- The new Zynq-7000 EPP Processing System provides developers with dozens of configuration options for memory, clocks, peripherals, DMA, IO, Interrupts and Flash memory interfaces. XPS now includes a new configuration window which enables users to graphically configure each parameter with guaranteed routing, voltage and clock-correct automated selections.
- 14.1 includes standard Zynq-7000 EPP configurations (for the ZC702 board), to enable developers to begin work immediately.
- The new Zynq-7000 EPP MIO summary window provides an aligned, color-coded graphic view of peripheral pin outs for faster, easier and guaranteed-correct MIO selection.

What's New in SDK?

- 14.1 now provides Xilinx SDK free of charge with all FlexLM license checks removed. SDK can be installed from a stand-alone installer (available on the Xilinx website) or within each ISE design tools edition installation.
- Full support for Zynq-7000 EPP
 - SDK now provides a full tools solution for bare-metal and Linux application development and profiling. Such tools include ARM GCC updated for bare-metal (EABI) and Linux development, Boot Image Creator, Flash programmer for QSPI, Device tree generator, and the remote system explorer (debug an IP-connected target board).
 - SDK works with XPS to build and generate design-specific firmware including the first stage boot loader with provision for device security, fallback boot, and bitstream management. It will also combine, build and deploy a complete bootable system image to the Zynq-7000 EPP target platform.

ChipScope Pro Tool and iMPACT

- Zynq-7000 EPP
 - Indirect Quad-SPI Flash programming support via iMPACT
 - ChipScope™ Pro tool device programming and debug support
 - iMPACT basic and advanced programming support
- Virtex-7 FPGA
 - IBERT 2-D Eye Scan enhancements
 - 7 series FPGA GTH support
 - ChipScope Pro tool device programming and debug support
 - iMPACT basic and advanced programming support
- Kintex-7 FPGA
 - IBERT 2-D Eye Scan enhancements
 - ChipScope Pro tool device programming and debug support
 - iMPACT basic and advanced programming support
- Artix-7 FPGA
 - Core generator and inserter support
- ChipScope Pro tool AXI Monitor now supports EDK and standard CORE Generator tool flows

System Generator for DSP

- Device support updated to include Defense-Grade 7 Series FPGA and Automotive XA Zynq-7000 EPP families
- PlanAhead design tool integration
 - Integrate System Generator modules in a larger RTL design
 - Includes tutorial
- New “Performance Tips” toolbar button which opens “High Performance Designs” documentation
- Blockset enhanced with FIFO support for embedded register in BRAM configuration

IBIS Simulation

- 7 series FPGA IBIS support is provided only through the PlanAhead design tool `write_ibis` command

- IBISWriter is not available for 7 series FPGA Families

Partial Reconfiguration

- Device support updated to include the XC7VX980T, XC7A200T, and XC7A350T.
 - Bitstream generation for Artix-7 devices is disabled in 14.1
- The list of resources that must remain static-only has been updated to include IO and configuration components.

Intellectual Property (IP)

Device Support

- Pre-production support has been added for the following families:
 - Defense-Grade Virtex-7Q FPGA
 - Defense-Grade Kintex-7Q FPGA
 - Defense-Grade Artix-7Q FPGA
 - XA Artix-7 FPGA
 - XA Zynq-7000 EPP

New IP Cores

- SMPTE 2022 5/6 Video over IP v1.0 - provides Transmitter and Receiver cores for broadcast applications that require bridging between Broadcast Connectivity standards (SD/HD/3G) and 10G networks.
- Ten Gigabit Ethernet 10GBASE-KR – 10G Ethernet PCS/PMA with optional Forward Error Correction (FEC) and Auto-Negotiation (AN) for 7 series FPGA GTX and GTH transceivers. Delivered as an optional, separately licensed configuration of the Ten Gigabit Ethernet PCS/PMA (10GBASE-R/KR) IP core.
- Asynchronous Sample Rate Converter for Digital Audio - converts stereo audio from one sample frequency to another. The input and output sample frequencies can be either an arbitrary fraction of each another, or the same frequency, but based on different clocks.
- Video In to AXI4-Stream - converts common parallel clocked video signals to an AXI4-Stream interface. This enables connection of external video sources such as a DVI PHY to other video processing blocks that use the AXI4-Stream interface (for example Xilinx Video IP).
- AXI4-Stream to Video Out - converts AXI4-Stream interface signals to a standard parallel video output interface with timing signals. This enables connection of video

processing blocks that use the AXI4-Stream interface (for example Xilinx Video IP) to external video sinks such as DVI PHY.

- AXI4-Stream Interconnect - a key interconnect infrastructure IP that simplifies the process of connecting heterogeneous master/slave AMBA® AXI4-Stream protocol compliant endpoint IP. The core routes connections from one or more AXI4-Stream master channels to one or more AXI4-Stream slave channels.
- AXI Performance Monitor - measures major performance metrics for the AMBA Advanced eXtensible Interface (AXI) system. Metrics supported include bus latency of a specific master/slave (AXI4/AXI4-Lite/AXI4-Stream) in a system, and the amount of memory traffic during specific periods of time.

Virtex-7 FPGA GTH Transceiver Support

- Pre-production Virtex-7 FPGA GTH support has been added to these IP Cores:
 - Ten Gigabit Ethernet 10GBASE-KR
 - 10GBASE-R
 - RXAUI
 - XAUI
 - QSGMII
 - 1000BASE-X/SGMII

Updates to existing IP versions

- FIFO Generator v9.1
 - Maximum data width increased to 4096 for AXI FIFO configurations
- 7 Series FPGA Transceiver Wizard (GT Wizard) v2.1
 - New example design module for GTX and GTH transceivers demonstrates the initialization sequence described in UG769.
 - Port and Attribute settings updated to support Initial ES (IES) GTH devices
 - New GTX Protocol templates (simulation only): HD-SDI, 3G-SDI, 6G-SDI and PCI Express Gen1, Gen2
 - New GTH Protocol templates (simulation only): XAUI, RXAUI, OTL3.4, OC48, Gigabit Ethernet (1000BASE-X PCS/PMA), QSGMII, CPRI, PCI Express Gen1, Gen2
 - New GTP Protocol templates (simulation only): DisplayPort, CPRI, Gigabit Ethernet (1000BASE-X PCS/PMA), QSGMI, V-by-One, HD-SDI, 3G-SDI, 6G-SDI, RXAUI, XAUI
- DisplayPort v3.1

- 5.4Gbps Single Stream transport (SST) support for 7 series FPGA devices from Specification version 1.2
- Luminance-only mode for Gray scale video users
- Parameterized Bits Per Component (BPC) to reduce memory footprint
- Quad pixel-wide video clock interface
- Secondary Audio (2-channel) option (separately licensed)
- AXI Bus Functional Model (AXI BFM) v2.1
 - Added VHDL examples
 - Support for Synopsys VCS® and Aldec Riviera-PRO™ simulation tools

AXI4 IP & More Information

In general, the AXI4 interface is supported by the latest version of an IP for Zynq-7000 EPP & Virtex-7, Kintex-7, Virtex-6 and Spartan®-6 FPGA device families. Older “production” versions of IP continue to support the legacy interface for the respective core on Virtex-6, Spartan-6, Virtex-5, Virtex-4, and Spartan-3 device families only.

- The latest versions of CORE Generator tool IP have been updated with Production AXI4 interface support. For more details AXI IP support information see http://www.xilinx.com/ipcenter/axi4_ip.htm.
- For general information on AXI4 support, see <http://www.xilinx.com/ipcenter/axi4.htm>.
- For a comprehensive listing of IP cores in the 14.1 release, please see http://www.xilinx.com/ipcenter/coregen/updates_14_1_2012_1.htm.
- For more information on IP New Features and Known Issues, refer to the IP Release Notes Guide (XTP025): http://www.xilinx.com/support/documentation/ip_documentation/xtp025.pdf.

Architecture Support and Requirements

Operating Systems

Xilinx only supports the following operating systems on x86 and x86-64 processor architectures.

Microsoft Windows Support

- Windows XP Professional (32-bit and 64-bit), English/Japanese
- Windows 7 Professional (32-bit and 64-bit), English/Japanese
- Windows Server 2008 (64-bit)

Linux Support

- Red Hat Enterprise Workstation 5 (32-bit and 64-bit)
- Red Hat Enterprise Workstation 6 (32-bit and 64-bit)
- SUSE Linux Enterprise 11 (32-bit and 64-bit)

Architectures

The following table lists architecture support for commercial products in the ISE Design Suite WebPACK tool vs. all other ISE Design Suite editions. For non-commercial support:

- All Xilinx Automotive devices are supported in the ISE Design Suite WebPACK tool.
- Xilinx Defense-Grade FPGA devices are supported where their equivalent commercial part sizes are supported.

Table 2-1: Architecture Support

	ISE WebPACK Tool	ISE Design Suite (All Other Editions)
Zynq EPP	Zynq-7000 EPP • XC7Z010, XC7Z020, XC7Z030	Zynq-7000 EPP • All
Virtex FPGA	Virtex-4 FPGA • LX: XC4VLX15, XC4VLX25 • SX: XC4VSX25 • FX: XC4VFX12 Virtex-5 FPGA • LX: XC5VLX30, XC5VLX50 • LXT: XC5VLX20T - XC5VLX50T • SXT: None • FXT: XC5VFX30T Virtex-6 FPGA • LXT: XC6VLX75T Virtex-7 FPGA • None	Virtex-4 FPGA • All Virtex-5 FPGA • All Virtex-6 FPGA • All Virtex-7 FPGA • All
Kintex FPGA	Kintex-7 FPGA • XC7K70T, XC7K160T	Kintex-7 FPGA • All
Artix FPGA	Artix-7 FPGA • XC7A100T, XC7A200T	Artix-7 FPGA • All
Spartan FPGA	Spartan-3 FPGA • XC3S50 - XC3S1500(L) Spartan-3A/-3AN/-3E FPGA • All Spartan-3A DSP FPGA • XC3SD1800A Spartan-6 FPGA • XC6SLX4 - XC6SLX75T	Spartan-3 FPGA • All Spartan-3A/-3AN/-3E FPGA • All Spartan-3A DSP FPGA • All Spartan-6 FPGA • All
CoolRunner™ XPLA3, CoolRunner-II, XC9500 CPLD	• All	• All

Compatible Third-Party Tools

Table 2-2: Compatible Third-Party Tools

Third-Party Tool	Red Hat Linux	Red-Hat Linux-64	SUSE Linux	Windows XP 32-bit	Windows XP-64 bit	Windows-7 32-bit	Windows-7 64-bit
Simulation							
Mentor Graphics ModelSim SE/DE (10.1a)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Mentor Graphics ModelSim PE (10.1a)	N/A	N/A	N/A	Yes	Yes	Yes	Yes
Mentor Graphics Questa® Advanced Simulator(10.1a)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Cadence Incisive® Enterprise Simulator (IES) (11.1)	Yes	Yes	Yes	N/A	N/A	N/A	N/A
Synopsys VCS® and VCS MX (F-2011.12)	Yes	Yes	Yes	N/A	N/A	N/A	N/A
The MathWorks MATLAB® and Simulink® with Fixed-Point Toolbox (2011a, 2011b)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Synthesis							
Synopsys Synplify®/Synplify Pro (F-2012.03-SP1)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Mentor Graphics Precision® RTL/Plus (2012a)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Equivalence Checking							
Cadence Encounter® Conformal® (9.1)	Yes	Yes	Yes	N/A	N/A	N/A	N/A

System Requirements

This section provides information on system memory requirements, cable installation, and other requirements and recommendations.

System Memory Recommendations

For memory recommendations for ISE Design Suite 14, see:

<http://www.xilinx.com/ise/products/memory.htm>

Operating Systems and Available Memory

The Microsoft Windows and Linux[®] operating system (OS) architectures have limitations on the maximum memory available to a Xilinx program. Users targeting the largest devices and most complex designs may encounter this limitation. The ISE Design Suite has optimized memory and enabled support for applications to increase RAM memory available to Xilinx tools.

Windows XP Professional 32-bit

Xilinx applications are enabled to take advantage of the memory increase feature on Windows 32-bit systems. You must then modify Windows setting to get access to this larger memory.

The standard Windows OS architecture limits the maximum memory available to a Xilinx process to 2 Gigabyte (GB). In Windows XP Professional, Microsoft created an option to support the ability of an application to address 3 GB of RAM. Xilinx ISE tools have built-in support for this option. To take advantage of this capability, you must also modify your Windows XP OS to enable this feature, which requires that you modify your `boot.ini` file by adding a `/3GB` entry to the end of the `startup` line.

Before enabling 3 GB support for Xilinx applications, read the Microsoft Knowledge Base Article #328269 at <http://support.microsoft.com/?kbid=328269>. If you upgrade your computer to Windows XP Service Pack 1 (SP1) and you are using the `/3GB` switch, Windows may not restart without a patch from Microsoft. See the Xilinx Answer Record 17905 for more information at <http://www.xilinx.com/support/answers/17905.htm>.

Additionally, before making this change, read:

- Microsoft Bulletin Q17193 <http://support.microsoft.com/default.aspx?scid=kb;en-us;Q171793>, which contains information on "Application Use of 4GT RAM Tuning".
- Microsoft Bulletin Q289022 <http://support.microsoft.com/default.aspx?scid=kb;en-us;q289022>, which contains instructions for editing your `boot.ini` file.

Linux

For 32-bit Red Hat Enterprise Linux systems, the operating system can use the `hugemem` kernel to allocate 4 GB to each process. More information can be found on the Red Hat support site: <http://www.redhat.com/docs/manuals/enterprise/>

Cable Installation Requirements

Platform Cable USB II and Parallel Cable IV are high-performance cables that enable Xilinx® design tools to program and configure target hardware.

To install Platform Cable USB II, a system must have at least a USB 1.1 port. For maximum performance, Xilinx recommends using Platform Cable USB II with a USB 2.0 port.

To install Parallel Cable IV, a system must have a parallel port connector and support parallel port communication.

Cables are officially supported on the 32-bit and 64-bit versions of the following operating systems: Windows XP Professional, Windows-7, Red Hat Linux Enterprise, and SUSE Linux Enterprise 11. Additional platform specific notes are as follows:

- Root privileges are required.
- SUSE Linux Enterprise 11: The fxload software package is required to ensure correct Platform Cable USB II operation. The fxload package is not automatically installed on SUSE Linux Enterprise 11 distributions, and must be installed by the user or System Administrator.
- Linux LibUSB support: Support for Platform Cable USB II based upon the LibUSB package is now available from the Xilinx website. See Xilinx Answer Record 29310 at: <http://www.xilinx.com/support/answers/29310.htm>.

For additional information regarding Xilinx cables, refer to the following documents:

- USB Cable Installation Guide (UG344): http://www.xilinx.com/support/documentation/user_guides/ug344.pdf
- Platform Cable USB II Data Sheet (DS593): http://www.xilinx.com/support/documentation/data_sheets/ds593.pdf
- Parallel Cable IV Data Sheet (DS097): http://www.xilinx.com/support/documentation/data_sheets/ds097.pdf

Equipment and Permissions

The following table lists related equipment, permissions, and network connections.

Table 2-3: Equipment and Permissions Requirements

Item	Requirement
Directory permissions	Write permissions must exist for all directories containing design files to be edited.
Monitor	16-bit color VGA with a minimum recommended resolution of 1024 by 768 pixels.

Item	Requirement
Drive	You must have a DVD-ROM for ISE Design Suite (if you have received a DVD, rather than downloading from the web).
Ports	<p>To program devices, you must have an available parallel, or USB port appropriate for your Xilinx programming cable. Specifications for ports are listed in the documentation for your cable.</p> <p>Note: Installation of the cable driver software requires Windows XP Pro SP1 (or later), or Windows-7. If you are not using one of these operating systems, the cables may not work properly.</p>

Note: X Servers/ Remote Desktop Servers, such as Exceed, ReflectionX, and XWin32, are not supported.

Network Time Synchronization

When design files are located on a network machine, other than the machine with the installed software, the clock settings of both machines must be set the same. These times must be synchronized on a regular basis for continued proper functioning of the software.

Technical Support and Documentation

Known Issues

ISE Design Suite Tools Known Issues can be found at the following Xilinx Answer Record:
<http://www.xilinx.com/support/answers/46491.htm>.

Support Site

For general technical questions, visit the Xilinx Product Support and Documentation site at <http://www.xilinx.com/support/>, where you can search the Answers Database or utilize other self-support features such as:

- Download Center, <http://www.xilinx.com/support/download/index.htm>
- Xilinx User Community Forums, <http://forums.xilinx.com>
- Free Design Training Videos, <http://www.xilinx.com/training/free-video-courses.htm>

If you cannot resolve your issue using our online resources, you can contact Xilinx Technical Support directly at <http://www.xilinx.com/support/techsup/tappinfo.htm>.

Customer Training

Xilinx hands-on training programs provide you with the foundational knowledge necessary to begin designing right away. These programs target both engineers new to FPGA technology and experienced engineers developing complex connectivity, digital signal processing, or embedded solutions.

For more information on training courses, free on-demand training, live online training, and upcoming events, visit the Xilinx Training website,
<http://www.xilinx.com/support/education-home.htm>.

Documentation

Context-Sensitive Help

Context-sensitive online Help is available for most ISE Design Suite tools that are available with a graphical user interface (GUI). From Project Navigator, select **Help > Help Topics** to access the online Help or press **F1**.

Software Manuals

Detailed software manuals about the ISE Design Suite tools and command-line functions are found on xilinx.com. To locate the Software Manuals on the website:

1. Go to the Documentation Center, <http://www.xilinx.com/support/>.
2. Click the **Design Tools** tab.
3. Click the Design Tool category and version, such as ISE tools 14.1, or click the **See All Design Tools Documentation** link.

Glossary

For a glossary of technical terms used in Xilinx documentation, see:
<http://www.xilinx.com/company/terms.htm>.

Third-Party Licenses

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