Pin Planning Methodology Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/2011	13.1	Initial version
07/06/2011	13.2	• Added additional information to first paragraph of main chapter regarding use of RTL project in the PlanAhead tool along with a synthesized netlist. • Added New Step 1: Select Device. • Changed Other IP to Connectivity IP. • Changed Noise Analysis to Noise Analysis (SSO and SSN). • Changed dual-purpose to multifunction. • Under Select Gigabit Transceivers, added information regarding placing GTs and avoiding use of hard IP. • Under Define Memory Interfaces, added information regarding generated constraints file. • Under I/O Interfaces, added information regarding creating interface groups in the PlanAhead tool to manage additional interfaces. • Under I/O Standards, Attributes, added information regarding unplaced pins and differential pairs. • Under Clock Pins and Topology, added information regarding viewing package from top or bottom, and information on PCB design recommendations and pin planning guidelines. • Under Place and Route, added information regarding locking down pins s and running DRCs before place and route. • Under Noise Analysis (SSO and SSN), added descriptions of SSO and SSN. • Under Noise Analysis (SSO and SSN), changed Weighted Average Simultaneous Switching Output (WASSO) to Simultaneous Switching Output (SSO). • Added reference to *PCB Design and Pin Planning Guide*.
04/24/2012	14.1	• Added following to Step 1. Select Device: "For designs using Stacked Silicon Interconnect (SSI) technology, see the *Large FPGA Methodology Guide (UG782)* cited in Appendix A, Additional Resources."

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Pin Planning Methodology

The *Pin Planning Methodology Guide* recommends an Input/Output (I/O) pin planning methodology for Xilinx® devices using the Xilinx PlanAhead™ design analysis tool.

While you can do pin planning at any step in the flow, this guide focuses on an RTL project with a synthesized netlist that allows more Design Rules Checks (DRCs) to run.

If an RTL project and netlist is not available, the PlanAhead tool allows an alternate limited pin planning-only flow.

The PlanAhead tool and its I/O planning environment provide a design flow from Register Transfer Level (RTL) to bit stream. They allow you to:

- Create, import, and configure the initial list of I/O ports early in the design flow.
- Perform final verification of the pinout at the end of the design flow.
- Group related ports into interfaces, then assign them to package pins.
- Use fully automatic pin placement or semi-automated interactive modes for controlled I/O port assignment.
- View the relationship of the physical package pins and banks with their corresponding I/O die pads.
- Make intelligent decisions to optimize the connectivity between the PCB and the FPGA device.

I/O Pin Planning Methodology Steps

The I/O pin planning methodology recommended by Xilinx includes the following steps:

- Step 1. Select Device
- Step 2. Select Configuration Mode
- Step 3. Select Gigabit Transceivers
- Step 4. Define Memory Interfaces
- Step 5. Connectivity IP
- Step 6. I/O Interfaces
- Step 7. I/O Standards, Attributes
- Step 8. Clock Pins and Topology
- Step 9. Place and Route
- Step 10. Noise Analysis (SSN and SSO)
- Step 11. Board Level Considerations

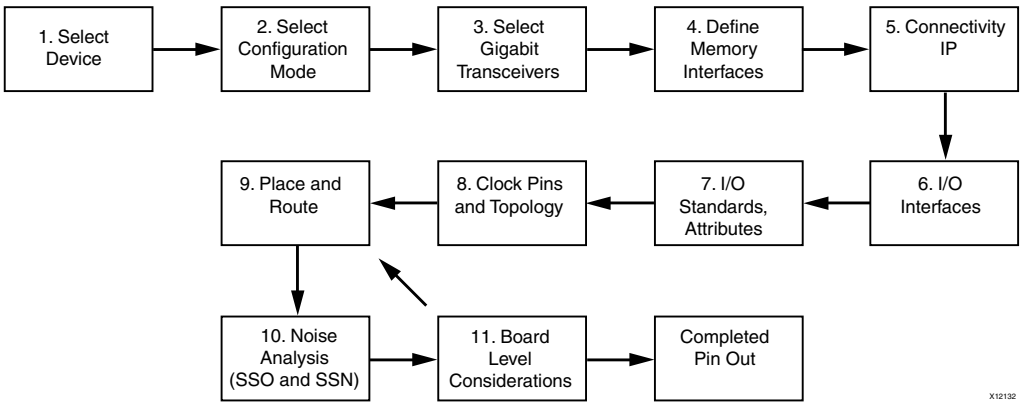

Figure 1-1: **Xilinx Recommended Pin Planning Methodology**

Step 1. Select Device

- Determine device size based on resource needs.

  For designs using Stacked Silicon Interconnect (SSI) technology, see the *Large FPGA Methodology Guide (UG782)* cited in Appendix A, Additional Resources.
- Select package and possible alternative packages based on PCB requirements such as critical routes to memories.

Step 2. Select Configuration Mode

- Most configuration modes share some pins with User I/O. The number of shared pins typically is *none* to *small* for serial modes, and grows larger for parallel modes.
- Avoid signal contention to ensure successful configuration. If I/O components are used after configuration, they must be changed to tristate during configuration.
- If the design allows, prohibit all multifunction pins to simplify the pinout.

- For more information, see the *Configuration User Guide* for each device family cited in Appendix A, Additional Resources. The guides describe the dedicated and shared configuration pins for each mode. Check the user guide to see if certain configuration modes create additional pinout restrictions.

Step 3. Select Gigabit Transceivers

- Gigabit Transceivers (GTs) have a set of dedicated pins.
- GTs typically share clock pins with other GTs or I/O clock regions.
- Adjacent to the GTs, most device families list which user I/O components to avoid in order to achieve optimal signal integrity.
- Use the Clock Resources and Device views to help place GTs. Hard IP (such as PCIe) in a device can block a GT and should be avoided.
- For more information, see the *Gigabit Transceivers User Guide* for each device family cited in Appendix A, Additional Resources.

Step 4. Define Memory Interfaces

- High speed memory interfaces have specific pinout requirements driven by clocking and skew needs.
- The Memory Interface Generator (MIG) tool generates the required pinouts.
- Ensure that the generated constraints file is added to your project.

Step 5. Connectivity IP

- Some Intellectual Property (IP) such as Ethernet and the PCIe® tool have specific pinout requirements.
- Use the Xilinx CORE Generator™ tool to incorporate any IP with external interfaces into the design.
- Like the Memory Interface Generator (MIG) tool, the CORE Generator tool generates the required pinout constraints.

Step 6. I/O Interfaces

- Define any additional I/O interfaces.
- Create interface groups in the PlanAhead tool to manage additional interfaces. Creating interface groups allows you to:
  - Simplify the ports list. You can group, place, manage and highlight interfaces as one object.
  - Give hierarchy to the ports list.

Step 7. I/O Standards, Attributes

- Define the I/O standards and other attributes.
- Place all unplaced pins so all pins are locked down. You can use the auto-placement feature to finish.
- Be conscious of differential pairs. In the Package view, you can enable and disable the Show Differential I/O Pairs option.
- Run a Design Rules Check (DRC) in the PlanAhead tool to check I/O standard versus I/O banking restrictions.
- Some I/O standards can be combined within a single bank and some cannot. For information on banking rules, see the *SelectIO Resource User Guides* cited in Appendix A, Additional Resources.
- For information on the packaging and pinout specifications for specific device families, see the Packaging and Pinout guides available from the Xilinx support website. See, for example, the *Virtex-6 FPGA Packaging and Pinout Specifications (UG365)* cited in Appendix A, Additional Resources.

Step 8. Clock Pins and Topology

- Use the dedicated external clock pins on the FPGA device for best clock performance.
- Understand I/O versus fabric clocking resources.
- Understand regional clock restrictions in the device family.
- Designs with fewer clocks than the number of global clock resources are usually simpler.
- For more complex clock structures, enter the clock tree and enough loads to run the early design through place and route for validation.
- Complex clock structures include designs with high clock counts that require either automatic or manual floor planning to utilize regional clocks
- To aid in clock planning, the PlanAhead tool displays a graphical representation of the available clock resources for the target device.
- The package can be viewed from either the top or the bottom. Sometimes it is helpful to flip the part.
- The information on PCB design recommendations and pin planning guidelines shows:
  - Connectivity
  - Available clock resources
- For more information on Clocking Resources, see the *Clocking Resources User Guide* for each device family cited in Appendix A, Additional Resources.

Step 9. Place and Route

- By this point, most if not all of the primary structures (I/O, IP, and Clocking) should be defined. The more primary structures that are defined and available, the more accurate are the associated DRCs.
- Lock down all pins.
- Run DRCs before place and route.

- Run the design through place and route to validate the pinout.
- Not all logic needs to be in place, only the primary structures that affect pinout.
- Fully implement the design in order to ensure a legal I/O pinout.
- Review the **`ngdbuild`** and **`map`** reports for I/O and clock-related messages.
- Only the place and route tools contain all sign-off DRCs on the final design and pinout.

Step 10. Noise Analysis (SSN and SSO)

Table 1-1: **Noise Analysis Methods (SSN and SSO) Supported in the PlanAhead Tool**

Method	Description	Supported Devices
Simultaneous Switching Noise (SSN)	Based on relative pin locations, SSN determines pins with excessive noise. You can move those pins to another location within the bank, or to another bank.	• Spartan®-6 • Virtex®-6
Simultaneous Switching Output (SSO)	SSO calculates the maximum number of user I/O components that can be assigned within a bank. SSO does not take relative pin locations into account.	• Spartan-3 • Virtex-4 • Virtex-5 • Xilinx 7 series FPGA devices

Improving Results

To improve results when a violation occurs:

- Use I/O standards that have a lower noise impact for the failing group.
- Reduce noise by changing to a:
  - Lower drive strength
  - Parallel-terminated DCI I/O standard
  - Lower class of driver

  Example: Changing the SSTL Class II to an SSTL Class I.
- Relocate the pin within the bank to an alternate location that is a greater distance from other noisy pins.
- Spread the failing pins across multiple banks. This reduces the number of aggressive outputs on the power system of one bank.
- Spread the failing group across multiple synchronous phases.

Design Changes

If the design changes, do the following:

- Rerun Step 9. Place and Route.
- Return to Step 10. Noise Analysis (SSN and SSO).

For more information, see the *PlanAhead User Guide (UG632)* cited in Appendix A, Additional Resources.

Step 11. Board Level Considerations

- For board-level validation, perform signal integrity analysis using IBIS (Input/Output Buffer Information Specification) or HSPICE models.
- To optimize the pinout within the context of the entire board, import the FPGA pinout into third party products such as:
  - *Cadence Allegro FPGA System Planner*
  - Mentor Graphics I/O Designer
- If the pinout changes, do the following:
  - Rerun Step 9. Place and Route.
  - Continue from that step on.

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Appendix A

Additional Resources

Xilinx Resources

- ***Xilinx® Design Tools: Installation and Licensing Guide*** *(UG798)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/iil.pdf
- ***Xilinx Design Tools: Release Notes Guide*** *(UG631)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/irn.pdf
- **Xilinx Glossary**: http://www.xilinx.com/company/terms.htm
- **Product Support and Documentation**: http://www.xilinx.com/support/documentation/index.htm
- **Xilinx Device User Guides**: http://www.xilinx.com/support/documentation/user_guides.htm
- **Xilinx Data Sheets:** http://www.xilinx.com/support/documentation/data_sheets.htm

ISE Documentation

- ***Command Line Tools User Guide*** *(UG628)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/devref.pdf
- ***Constraints Guide*** *(UG625)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/cgd.pdf
- ***Timing Closure User Guide*** *(UG612)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/ug612.pdf
- ***Xilinx Synthesis and Simulation Design Guide*** *(UG626)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/sim.pdf
- ***XST User Guide for Virtex®-4, Virtex-5, Spartan®-3, and Newer CPLD Devices*** *(UG627)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/xst.pdf
- ***XST User Guide for Virtex-6, Spartan-6, and 7 Series Devices*** *(UG687)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/xst_v6s6.pdf
- ***Large FPGA Methodology Guide (UG782)***, http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/ug872_largefpga.pdf

PlanAhead Design Analysis Tool Documentation

- **PlanAhead Design Analysis Tool Documentation**: http://www.xilinx.com/support/documentation/dt_planahead_planahead/14-1_userguides.htm

- **User Guides**
  - ***PlanAhead User Guide*** *(UG632)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/PlanAhead_UserGuide.pdf
  - ***PlanAhead Tcl Command Reference Guide (UG789):*** http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/ug789_pa_tcl_commands.pdf
- **Methodology Guides**:
  - ***Floorplanning Methodology Guide*** *(UG633)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/Floorplanning_Methodology_Guide.pdf
  - ***Hierarchical Design Methodology Guide*** *(UG748)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/Hierarchical_Design_Methodology_Guide.pdf
- **Tutorials:** http://www.xilinx.com/support/documentation/dt_planahead_planahead14-1_tutorials.htm
  - ***Design Analysis and Floorplanning*** *(UG676)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/PlanAhead_Tutorial_Design_Analysis_Floorplan.pdf
  - ***I/O Pin Planning*** *(UG674)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/PlanAhead_Tutorial_IO_Pin_Planning.pdf
  - ***Leveraging Design Preservation for Predictable Results*** *(UG747):* http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/PlanAhead_Tutorial_Design_Preservation.pdf

Pin Planning Documentation

- For information on I/O pin planning and flows in the PlanAhead tool, see the *PlanAhead Software Tutorial - I/O Pin Planning (UG674)* at: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/PlanAhead_Tutorial_IO_Pin_Planning.pdf
- For information on the packaging and pinout specifications for specific device families, see the Packaging and Pinout guides available from the Xilinx support website. See, for example:
  - *Virtex-6 FPGA Packaging and Pinout Specifications (UG365)* at: http://www.xilinx.com/support/documentation/user_guides/ug365.pdf
- For information on banking rules, see the *SelectIO Resources User Guides* available from the Xilinx support website. See, for example:
  - *7 Series FPGAs SelectIO Resources User Guide (UG471)* at: http://www.xilinx.com/support/documentation/user_guides/ug471_7Series_SelectIO.pdf
- For information on PCB design recommendations and pin planning guidelines, see the *PCB Design and Pin Planning Guide* for each device family. See, for example:
  - *Spartan-6 FPGA PCB Design and Pin Planning Guide (UG393)* at: http://www.xilinx.com/support/documentation/user_guides/ug393.pdf
  - *7 Series FPGAs PCB Design and Pin Planning Guide (UG483)* at: http://www.xilinx.com/support/documentation/user_guides/ug483_7Series_PCB.pdf
- For information on PlanAhead functionality and commands, see "I/O Pin Planning" in the *PlanAhead User Guide (UG632)* at:

http://www.xilinx.com/support/documentation/dt_planahead_planahead/14-1_userguides.htm

- For information on configuration mode, see the *Configuration User Guide* for each device family available from the Xilinx support website at: http://www.xilinx.com/support/documentation
- For information about Gigabit Transceivers, see the *Gigabit Transceivers User Guide* for each device family available from the Xilinx support website at: http://www.xilinx.com/support/documentation
- For more information on Clocking Resources, see the *Clocking Resources User Guide* for each device family available from the Xilinx support website at: http://www.xilinx.com/support/documentation
- For information on the following third party pin planning tools that support Xilinx FPGA pin planning at the board level, see:
  - *Cadence Allegro FPGA System Planner (FSP)* at:

    www.cadence.com
  - *Mentor Graphics I/O Designer* at:

    www.mentor.com