Design Preservation Tutorial

PlanAhead Design Tool

UG747 (v14.5) April 25, 2013

XILINX®

Revision History

Date	Version	Revision
04/25/2013	14.5	Validated with Release.

Table of Contents

Design Preservation Tutorial

This tutorial provides an overview of the design preservation flow. In this tutorial, you will:

- Define partitions and Pblocks on an elaborated Register Transfer Level (RTL) design.
- Synthesize using the Xilinx® Synthesis Technology (XST) incremental synthesis software.
- Implement the partitioned design.
- Promote successful implementation results.
- Update the top-level partition.
- Rerun synthesis and implementation on the modified top level while importing the unchanged partitions.

The objective of this tutorial is to familiarize you with the partitions and the design preservation flow using the PlanAhead design tool. Many of the PlanAhead tool analysis features are covered in more detail in other tutorials, and not every command or command option is covered.

Tutorial Design Description

The design used throughout this tutorial contains:

- A RISC processor
- FFTs
- Gigabit transceivers
- Two USB port modules (to be partitioned)
- An xc6vlx75t device

A small design is used to allow the tutorial to be run with minimal hardware requirements and to enable timely completion, as well as to minimize the data size.

Software Requirements

The PlanAhead tool is installed with ISE Design Suite software. Before starting the tutorial, be sure that the PlanAhead tool is operational, and that the tutorial design data is installed.

For installation instructions and information, see the *ISE Design Suite 14: Release Notes, Installation, and Licensing (UG631)*.

Hardware Requirements

Xilinx recommends a minimum of 2 GB of RAM when using the PlanAhead tool on larger devices. For this tutorial, a smaller design is used, and the number of designs open at one time is limited. Although 1 GB is sufficient, it can impact performance.

Preparing the Tutorial Design Files

This tutorial uses a reference design, **PlanAhead_Tutorial_DP.zip**, which you can download from the Xilinx PlanAhead Tutorials web page at:

http://www.xilinx.com/cgi-bin/docs/rdoc?v=14.5;t=planahead+tutorials

Extract the zip file contents into any write-accessible location. The extraction directory will be referred to in this tutorial as <*Extract_Dir*>.

RECOMMENDED: *The tutorial sample design data is modified while performing this tutorial. A new copy of the original PlanAhead_Tutorial data should be extracted each time you run this tutorial.*

This tutorial includes a project file that has already been implemented. To reduce the data size, some implementation files were removed from the design, leaving only the required results data in the run directories.

Lab 1: Design Preservation in PlanAhead

Step 1: Opening and Elaborating an RTL Project

This tutorial uses pre-existing PlanAhead tool projects to simplify the steps and focus on the design preservation aspects of the tutorial. For a real design, you would use the New Project Wizard to create either an RTL or netlist based project.

Opening an Existing RTL Project

To open an existing PlanAhead tool RTL project:

1. Open the PlanAhead tool.
   - On Windows, double-click the Xilinx® PlanAhead Desktop icon, or select:

     Start > All Programs > Xilinx Design Tools > ISE Design Suite 14.5 > PlanAhead > PlanAhead
   - On Linux, go to the `<Extract_Dir>` directory and type **PlanAhead**:
2. From the Getting Started page, click **Open Project**.
3. In the `<Extract_Dir>` directory, open the project file located at:

   `./Projects/project_DP_RTL/project_DP_RTL.ppr`

Viewing Source Files

When the project opens, the Project Manager view is visible. You can view the following design files in the Sources window:

- VHDL source files
- Verilog source files
- A User Constraints File (UCF) named `top_full.ucf`. This file contains timing constraints and I/O pin locations.

Elaborating an RTL Design

You must use the Elaborated Design view to define partitions in an RTL project. When the Elaborated Design view is opened:

- The RTL code is elaborated.
- The design hierarchy is displayed.

Use this pre-synthesized view of the design to define partitions and create constraints.

To elaborate an RTL design:

1. Select **Flow > New Elaborated Design**, or click **Open Elaborated Design** in the Flow Navigator.

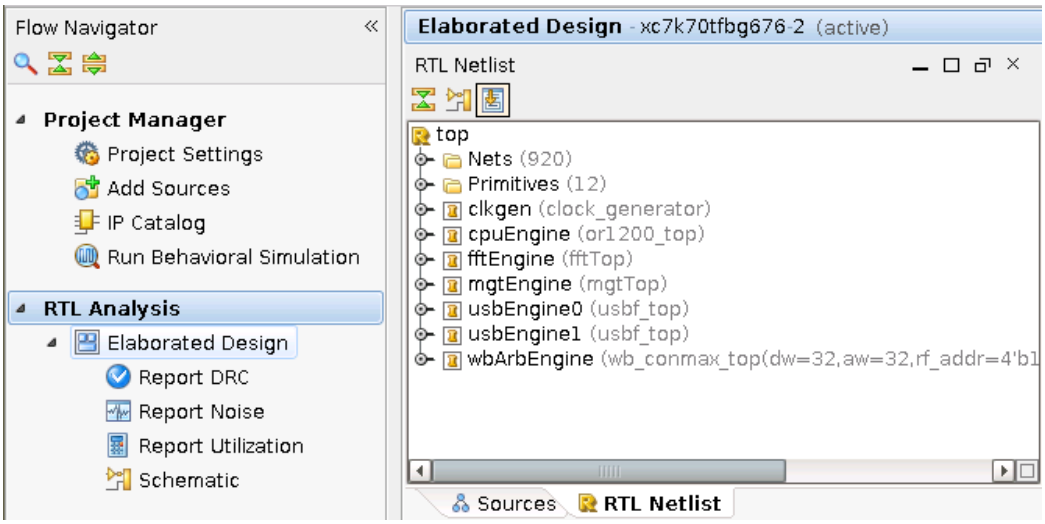

Figure 1: Opening the Elaborated Design view

Step 2: Setting Partitions and Drawing Pblocks

Because the **usbEngine** instances have already been identified as timing-critical modules, it would be advantageous to preserve the successful implementation results of these instances. However, this fact alone does not make these instances good candidates for partitions.

The **usbEngine** instances are good choices for partitions because:

- They are logically isolated from the rest of the design.
- They have reasonable interface timing (registered inputs and outputs).

Use DRCs to help identify whether or not a module is a good choice for partitions. For more information on how to choose good module instances for partitioning, see *the Hierarchical Design Methodology Guide (UG748)*.

You can floorplan partitioned instances like any other instances. Creating Pblock (AREA_GROUP) constraints can help achieve timing closure and improve runtime. The UCF provided with this tutorial constrains the I/O logic of the **usbEngine** along the left side of the device. The steps below show you how to create appropriate Pblock constraints for the two **usbEngine** instances.

Setting Partitions for the two usbEngine Instances

To set partitions for the two **usbEngine** instances:

1. From the RTL Netlist view, **select** the two **usbEngine** modules.
2. **Right-click** to open the **popup menu**, and select **Set Partition**.

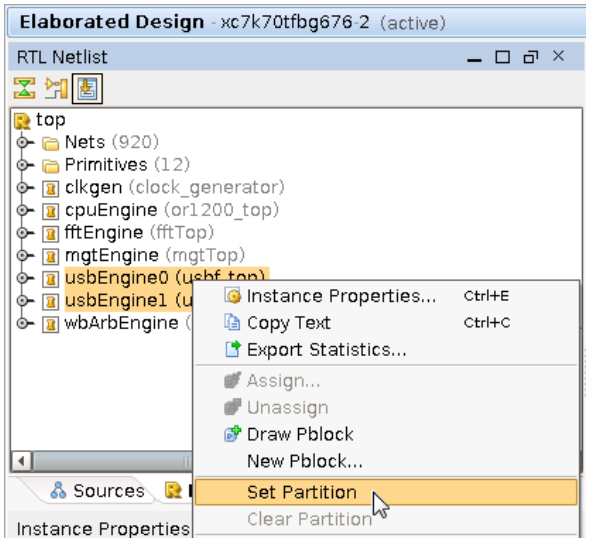

Figure 2: Setting Partitions on usbEngine Instances

Drawing Pblocks for the Two usbEngine Instances

This step does not affect synthesis results, so it could also be done post-synthesis in the Synthesized Design view. There are some advantages to doing so, such as resource estimation to help size the Pblocks. However, for this tutorial it will be done from the Elaborated Design view.

To draw Pblocks for the two **usbEngine** instances:

1. From the RTL Netlist window, select usbEngine1.
2. Right-click and select Draw Pblock.

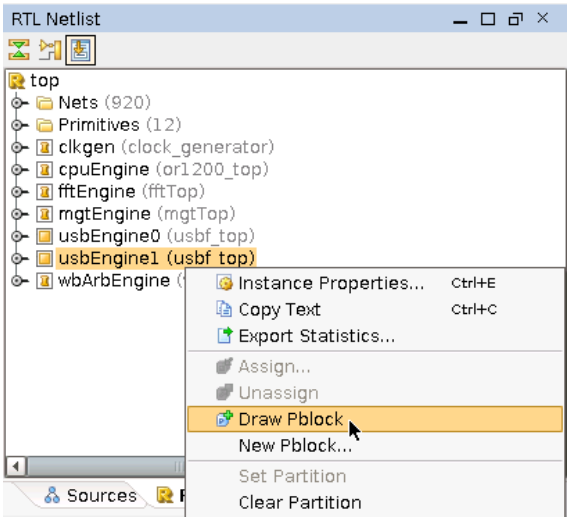

Figure 3: Selecting the Draw Pblock Tool

3. With the Draw Pblock tool active, move the cursor to the Device window.
4. Left click the top-left corner of the device where the CLB components start.
5. Without releasing the left mouse button, drag to create a rectangle covering most of the top-left quadrant of the device. See Figure 4.
6. In the New Pblock dialog box, verify that the SLICE and RAMB36 grids are selected.
7. Deselect other resources that are not needed, as shown in Figure 4.
8. Verify that the number of available RAMB36 components (shown in parentheses) is 40.

   If the rectangle does not fully cover the region shown in Figure 4, the number of available RAMB36 may be less, and the design may fail to place.

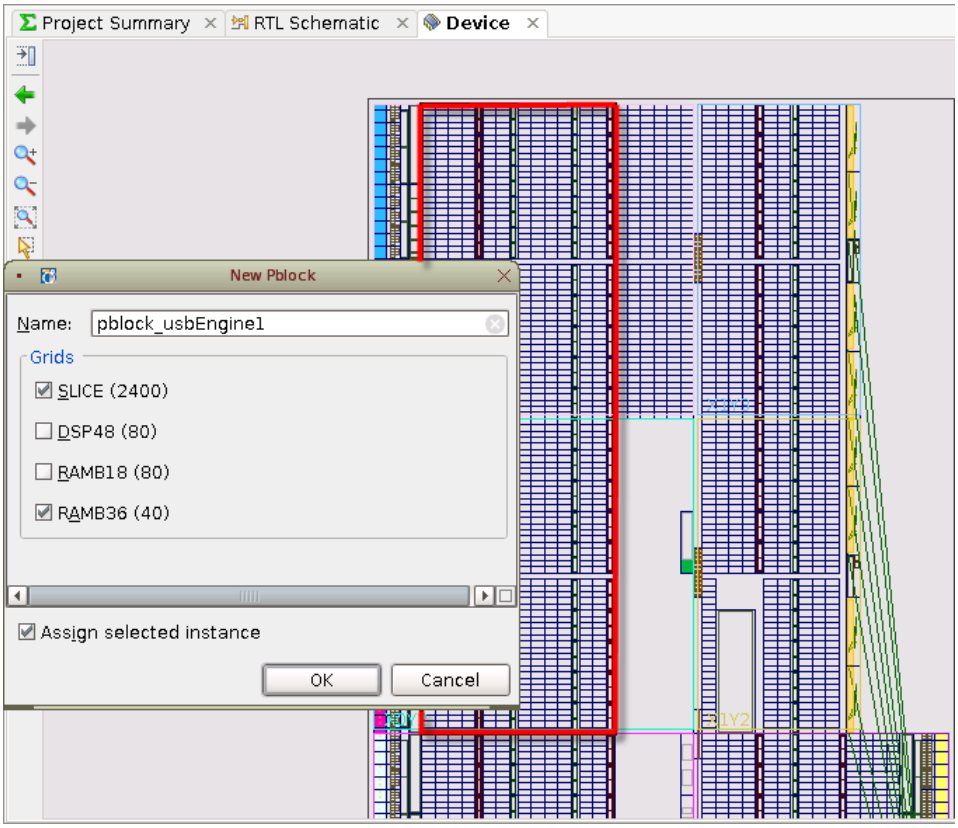

Figure 4: Pblock Rectangle for usbEngine1

9. Click **OK**.

10. Repeat the steps above for **usbEngine0** on the bottom-left quadrant. See Figure 5 for the final Pblock ranges.

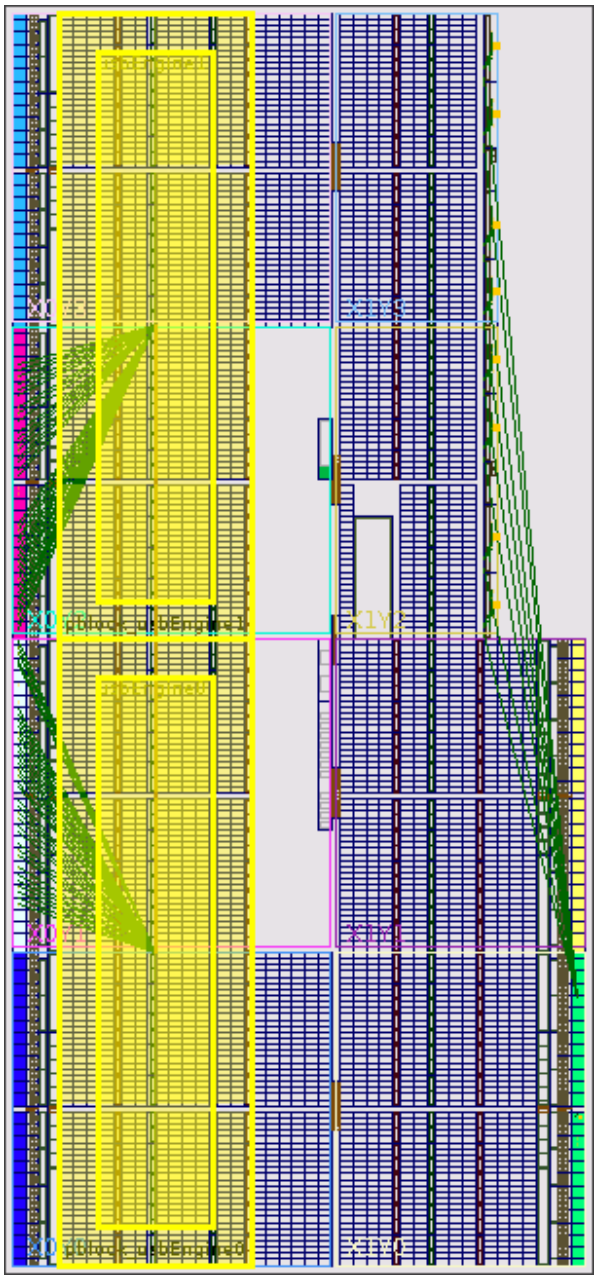

Figure 5: Completed Floorplan for Pblocks usbEngine0 and usbEngine1

Step 3: Synthesizing and Implementing the Design

Now that all partitions have been defined, and all necessary constraints have been created, you can run synthesis and implementation. Because partitions were defined in the elaborated Hardware Description Language (HDL) design, XST does the following:

- Detects the partitions
- Runs incremental flow
- Creates an individual NGC file for each defined partition

NGC Files

The individual NGC files for each defined partition are uniquely named. Unique naming allows multiple instances of a module to be synthesized with different parameters. In this case, synthesis generates the following NGC files in the `<project_name>.runs/synth_1` directory:

- `top.ngc`
- `usbEngine0#usbf_top.ngc`
- `usbEngine1#usbf_top.ngc`

Running Synthesis outside the PlanAhead tool

If you prefer a bottom-up synthesis, or a third party incremental synthesis flow, run synthesis outside the PlanAhead tool.

Use a PlanAhead netlist project instead of the RTL project shown in this tutorial.

Running Synthesis in the PlanAhead tool

To run synthesis in the PlanAhead tool:

1. First check the settings on the partitions. Click **Specify Partitions** under **Project Manager** in the Flow Navigator.

   The Specify Partitions dialog box defines the actions to be taken by the PlanAhead tool for each of the defined partitions during either synthesis or implementation. The top-level of the design is always one of the partitions in the design. You have also defined `usbEngine0` and `usbEngine1` as partitions.

   At this time, you will be synthesizing and implementing all partitions in the design, rather than importing the partitions results from a repository. For more information on creating and using partitions, refer to the Hierarchical Design Methodology Guide (UG633).

2. In the Specify Partitions dialog box, ensure that **all partitions** are set to **Implement**, and click **OK**.

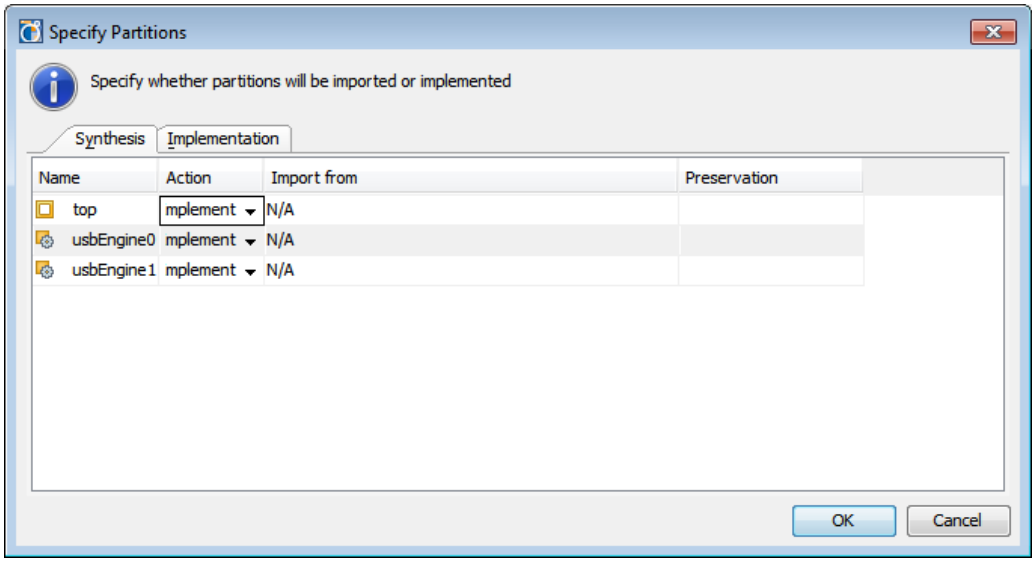

Figure 6: Specify Partitions

3. In the Flow Navigator, select **Run Synthesis**.
4. If prompted to save the design, select **Save**.

   Synthesis runs to completion, and the Synthesis Completed dialog box displays.
5. When the Synthesis Completed dialog box appears, select **Open Synthesized Design** and click **OK**.

Running a DRC on Partitions

While you can run a Design Rule Check (DRC) on the Elaborated Design, there are limitations on the parameters that the software can check at this stage. Xilinx recommends that you report DRC before launching implementation. To report DRC, load the Synthesized Design view and run partition-specific DRCs.

To report DRC on partitions:

1. Click **Synthesized Design** to open the view if not already open.

   Opening the Synthesized Design view loads the synthesis results and allows for additional DRC checking.
2. In the Flow Navigator under **Synthesized Design**, click **Report DRC** (or select **Tools > Report DRC**).
3. From the Report DRC dialog box, deselect all rules except **Partition**.

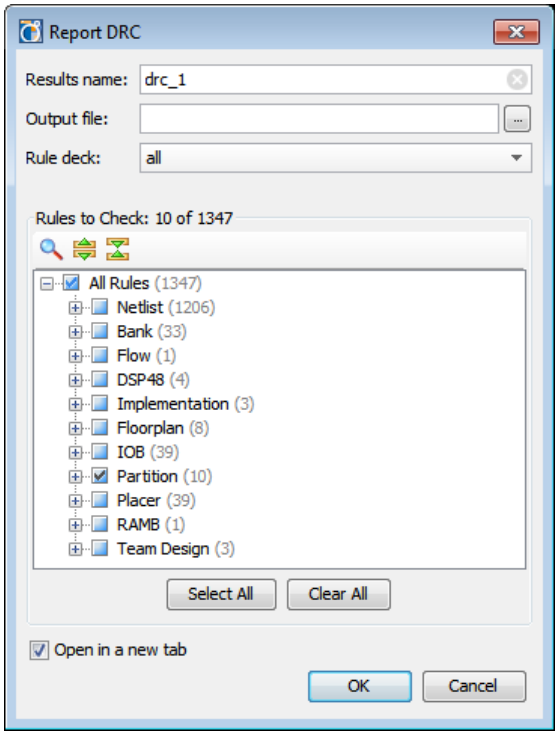

Figure 7: Report DRC

4. Click **OK**.

DRC Advisory Messages

The DRC returns minor Advisory messages. The PlanAhead tool can report the following message types for the DRC rules:

- Advisory
- Warning
- Error
- Fatal

Ignore the Advisory messages for this tutorial. In an actual design, investigate all DRC messages, and correct any serious issues.

Note: In an actual design, investigate all DRC messages, and correct any serious issues.

Running Implementation in the PlanAhead tool

You are now ready to run implementation in the PlanAhead tool. To implement this design with partitions, the only additional steps required were to:

- Define the partitions.
- Run a DRC check.

Because this design was already created with hierarchy in mind, you did not have to alter the design to make it work with partitions.

However, the bulk of the work required to make a partition design successful is at the RTL design stage, and not with the synthesis or implementation tools. For recommendations for good hierarchical design, see the *Hierarchical Design Methodology Guide (UG748)*.

Skipping Implementation

To remove the implementation runtime from this tutorial, a completed project with synthesis and implementation results can be found at:

```
<Extract_Dir>/Projects/project_DP_RTL_implemented
/project_DP_RTL_implemented.ppr
```

Close the current project and open the implemented project to skip ahead and open the implementation results. If you skip ahead, go to Step 4: Promoting Implemented Partitions.

Running Implementation

To run implementation in the PlanAhead tool:

1. In the Flow Navigator, click **Run Implementation**.
2. Click the **Report** tab to see a list of implementation reports. Each report is available as the process finishes.
3. After NGDBuild finishes, double-click **NGDBuild Report**.
4. Scroll to the bottom of the report to view the partition information, as seen in Figure 8.

   This partition information:

   - Appears in every report (NGDBuild, Map, and PAR)
   - Allows you to verify the status of all partitions on a given run easily

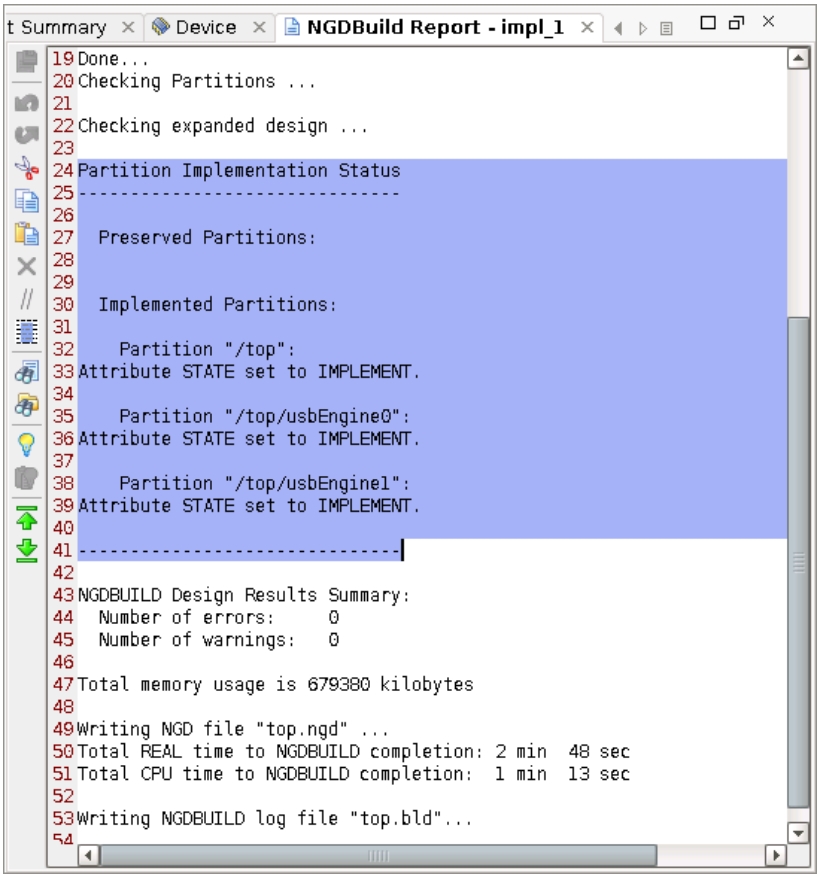

Figure 8: Implementation Status in Report Files

Step 4: Promoting Implemented Partitions

After the implementation has completed, you can promote the results for the partitions to a location to be later reused. Promoting the partition results makes a copy of the synthesis and implementation directory:

`<project_name>.promote\X<run_name>`

For example:

`project_DP_RTL.promote\Ximpl_1`

The PlanAhead tool:

- Keeps track of the latest promoted run.
- Changes the state and import location of any promoted partitions.

You can also manage these processes manually.

Promoting the Successful Implementation Results

After implementation has completed, the Implementation Completed dialog box opens.

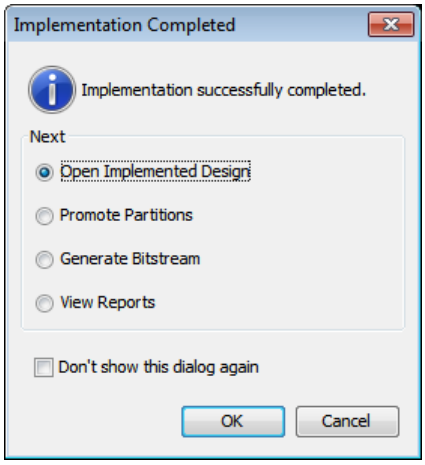

Figure 9: Implementation Completed Dialog Box

To promote the successful implementation results:

1. Select **Open Implemented Design** and click **OK**.

   Other options are also available. For example, you could promote the results by selecting Promote Partitions option. However, this tutorial uses another method to promote the results.

   Note: If the Implementation Completed dialog box did not open, or if you opened the completed project project_DP_RTL_implemented, load the results by clicking **Open Implemented Design** in the Flow Navigator.

To verify that the implementation results were successful, review the final timing score and the detailed timing, as seen in Figure 10.

- The timing score is **0**.
- The number of timing errors is **0**.

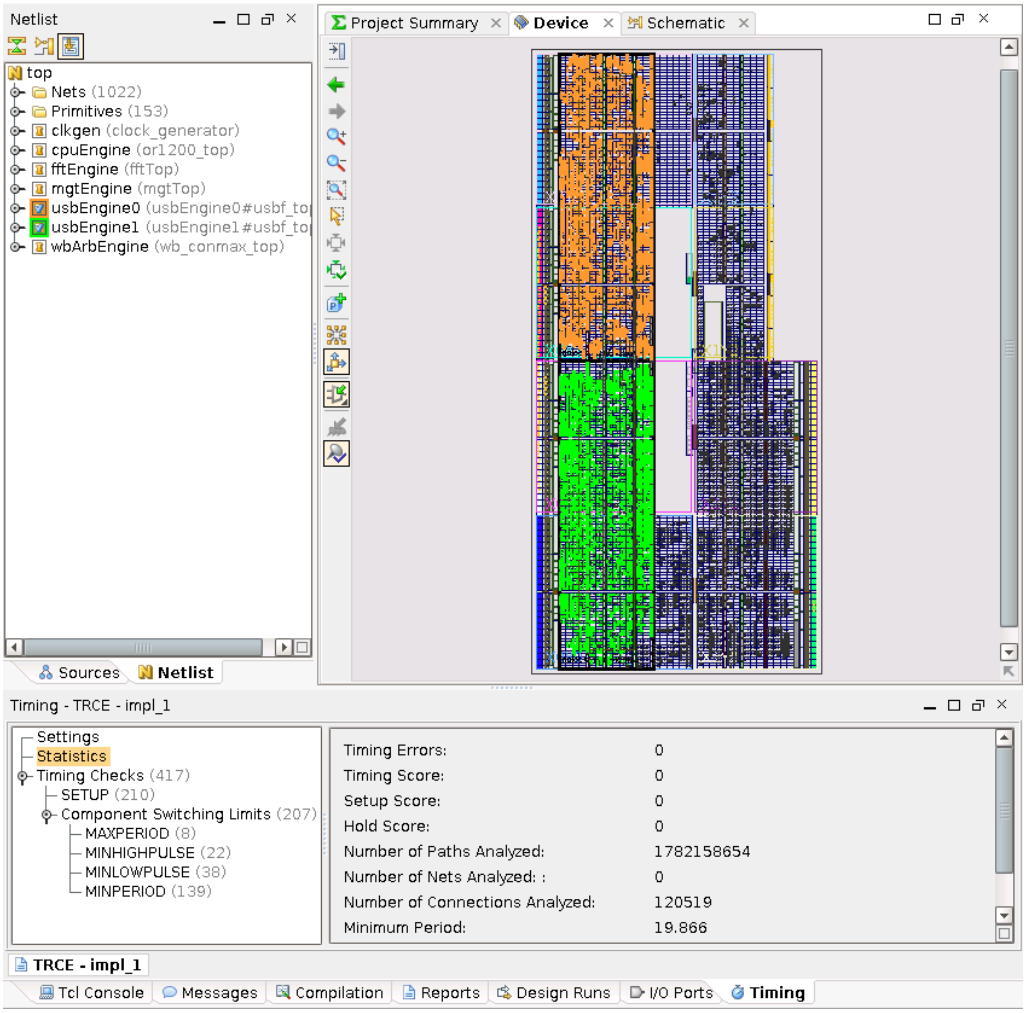

Figure 10: Verifying Successful Implementation Results

2. To highlight the primitives of the two **usbEngine** modules as shown in Figure 10:
   a) Select the two modules in the Netlist view.
   b) Right-click to open the popup menu.
   c) Select **Highlight Primitives > Cycle Colors**.

3. In the Flow Navigator, under Implementation, click **Promote Partitions.**

   This lets you promote the synthesis and implementation results for the defined partitions.

   Note: If the Elaborated Design view is not open you will be asked to open it when promoting partitions.

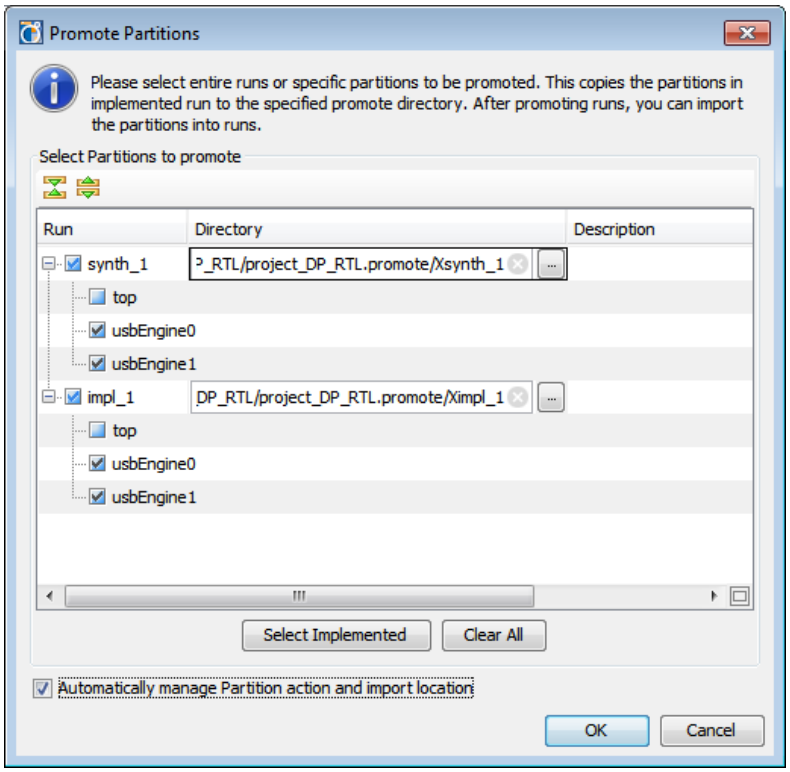

Figure 11: Promote Partitions Dialog Box

4. Verify that the two **usbEngine** module instances are checked for promoting for both synthesis and implementation, as shown in Figure 11.

   The top-level partition is not selected by default. However, you can promote this partition like any other partition. For this tutorial, since you update the top partition, there is no need to promote it now.

5. Add an optional **Description** for each of the partitions.

6. Verify that **Automatically manage Partition action and import location** is checked.

   Checking Automatically manage Partition action and import location allows the PlanAhead tool to track the state of the partition, and to automatically import results from subsequent synthesis and implementation runs. If this option is not checked, you must manage these tasks yourself.

7. Click **OK** to promote the partitions.

After promoting partitions into the current project, the Promoted Partitions view is opened, or can be opened by the **Windows > Promoted Partitions** command in the main menu. The Promoted Partitions view is shown in Figure 12.

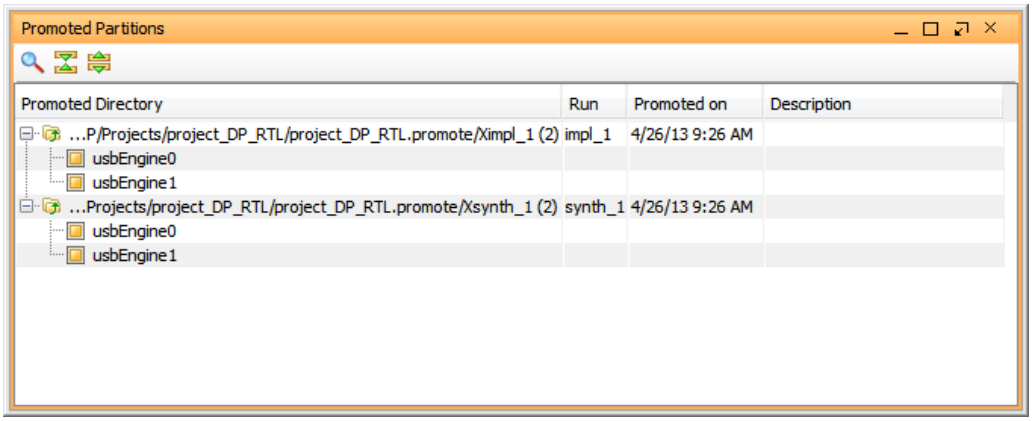

Figure 12: Promoted Partitions

Looking in the Specify Partitions dialog box now shows that the default action for the promoted partitions has been changed to Import.

The Specify Partitions dialog box can be accessed from the Project Manager section of the Flow Navigator, or from the Implemented Partitions section of the Project Summary.

Step 5: Modifying the RTL for Top

Now that you have promoted the synthesis and implementation results for the defined partitions, you will make a change to the design to update the partition. An example of such a change could be, for example, a new feature, a bug fix, or a pipeline register.

This tutorial makes a simple change to a module belonging to the top partition. You then re-synthesize and re-implement to update the changed partition, while preserving the two timing-critical **usbEngine** partitions.

Changing the Verilog File

1. Click **Project Manager** in the Flow Navigator to open the Project Manager view.
2. From the Hierarchy tab of the Sources view, expand the **Verilog Header** folder, and locate `or1200_defines.v` as shown in Figure 13.
3. Double-click `or1200_defines.v` to open it in the text editor.

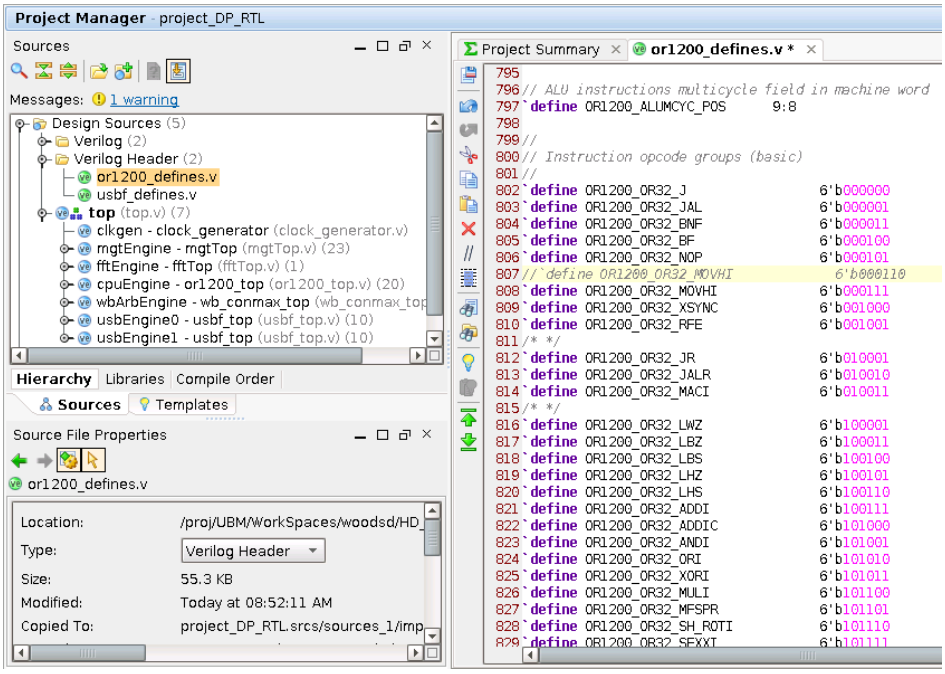

Figure 13: Updating or1200_defines.v

4. Insert two slashes (//) at the beginning of line 807, to comment out the line:

   ```
   //`define OR1200_OR32_MOVHI 6'b000110
   ```

5. Remove the two slashes (//) at the beginning of line 807, to uncomment the line:

   ```
   `define OR1200_OR32_MOVHI 6'b000111
   ```

6. In the **Text Editor**, right-click and select **Save File**, or click the Save File button.

When you save the changes to the `or1200_defines.v` file, the Synthesis & Implementation Out-of-Date status appears in the upper right hand corner of the current design.

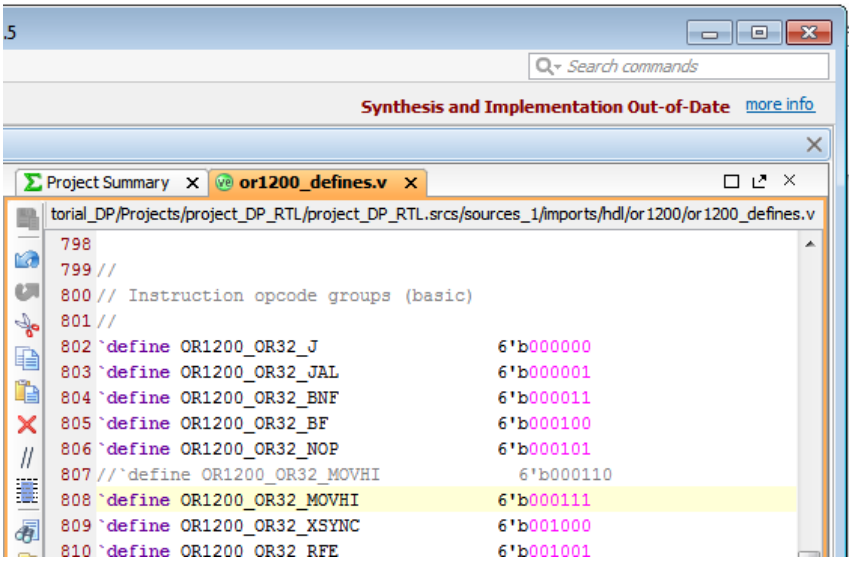

Figure 14: Synthesis and Implementation Out-of-Date

The PlanAhead tool recognizes that a source file has been modified, and that the current synthesis and implementation results may not reflect the latest version of the design. This status is intended to warn you that recent changes to the design may have made prior synthesis and implementation results obsolete. In this case, synthesis and implementation would need to be run again. You can click the more info link to see what is causing the out-of-date condition.

Note: In some case, you may have added a comment to a source file, or made a different minor change that does not actually affect synthesis or implementation. In this case, you can use the **Force Up-to-date** link to clear the out-of-date status.

Step 6: Rerunning Synthesis and Importing Partitions

Having changed the top-level design, you will now re-implement the design while preserving the results of the two usbEngine partitions.

First verify the actions associated with the various design partitions:

1. From the Flow Navigator, under Project Manager , click the **Specify Partitions** button.
2. **Verify** in both the **Synthesis** and **Implementation** tabs:
   - The top-level partition is set to Implement.
   - The two `usbEngine` partitions are set to Import.
3. Click **OK**.

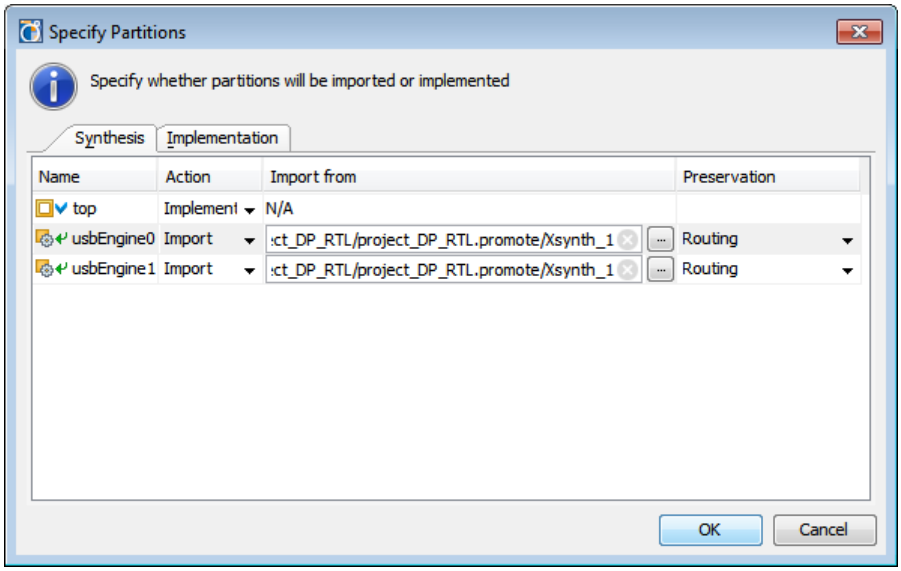

Figure 15: Verifying Partitions Attributes

Running Synthesis and Implementation

1. In the Flow Navigator, click **Run Implementation** to launch the implementation run.

   Because Synthesis is also out of date, you are prompted to launch synthesis first.
2. Click **Yes** to launch synthesis and implementation.
3. Review the Partition Status section in the NGDBuild, Map, and PAR reports to verify that:
   - The two **usbEngine** partitions are imported, and .
   - All timing constraints have been met.

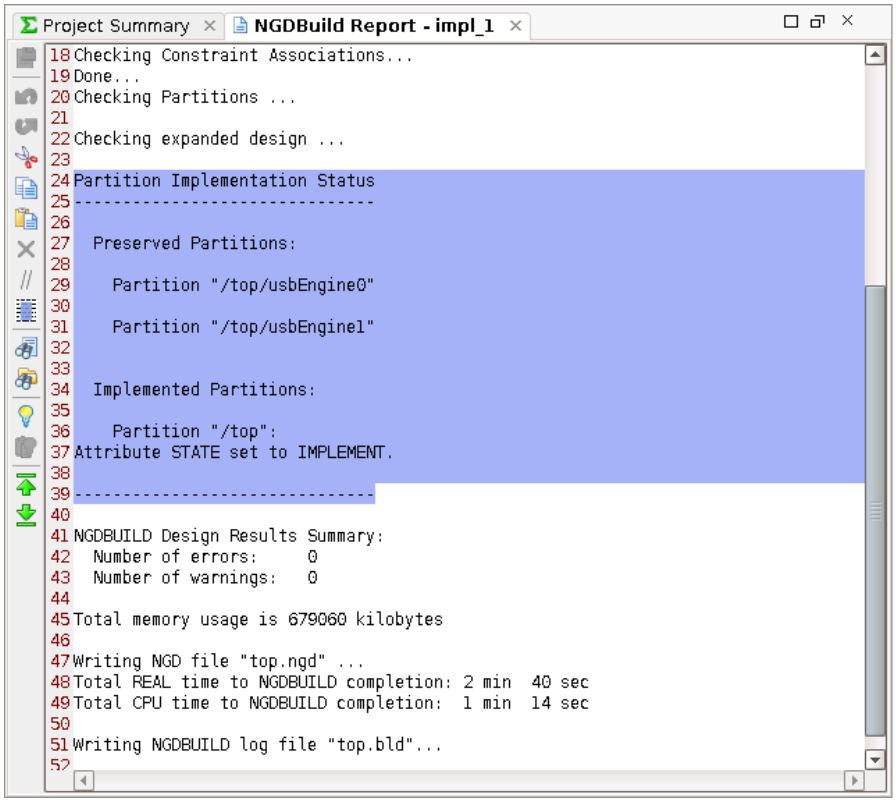

Figure 16: Partition Implementation Status in Report Files

Conclusion

In this tutorial, you did the following:

- Defined two usbEngine partitions,
- Defined Pblocks to constrain placement for these partitions,
- Synthesized and implemented the design,
- Promoted the two usbEngine partitions to preserve the results,
- Made a change to the top-level design,
- Re-synthesized and re-implemented the top-level design, and
- Imported the preserved results from the promoted partitions.

The preserved partitions helps guarantee timing results for two large, timing-critical modules in the current design. The design is preserved for all future iterations, or uses of the partition, assuming there are no changes to the **usbEngine** modules.