SDAccel Development Environment

Release Notes

UG1202 (v2016.2) September 15, 2016

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Changes
9/15/2016	2016.2	Introduces support for user control of kernel clock frequency for all DSAs. Support added for CentOS 7.2. Updated all examples to use Makefile flow. New DSA v3.1 for TUL TUL-PCIE3-KU115 and Alpha Data ADM-PCIE-8K5 **Note**: This is the last release to support Tcl script flow. Please update from Tcl script to Makefile flow using xocc.
6/14/2016	2016.1	Introduces higher kernel performance features for automatic loop pipelining and unrolling, memory coalescing and kernel clock scaling
2/16/2016	2015.4	Xilinx OpenCL runtime supports IBM Power8 Eclipse IDE enhanced with examples. Coding templates and performance optimization guide. New DSA v2.1 for Alpha Data ADM-PCIE-7V3 and ADM-PCIE-KU3 board. New DSA v2.1 for Alpha Data ADM-PCIE-7V3 with 1-DDR New DSA v2.1 for ADM-PCIE-KU3 board with 1-DDR and 2-DDR.
11/9/2015	2015.3	New DSA v2.0 for Alpha Data ADM-PCIE-7V3 Virtex-7 690T board and Alpha Data ADM-PCIE-KU3 Kintex® UltraScale® KU60 board. Beta release of Eclipse IDE with Debug, Profile and Application Trace.
6/1/2015	2015.1	Initial Xilinx 2015.1 release.

What's New

The SDAccel® Development Environment 2016.2 introduces support for user control of kernel clock frequency for FPGA accelerators and CentOS 7.2 support for development and application execution. The SDAccel release focuses on achieving higher kernel performance by introducing new features for automatic loop pipelining and unrolling, memory coalescing, and kernel clock scaling.

Note: Tcl script flow will not be supported in the next release of SDAccel. Please update from Tcl script to the Makefile flow using Xilinx command line compiler (xocc) with SDAccel 2016.2 release.

For examples of how to use xocc with Makefile flow, refer to the examples shipped with SDAccel 2016.2 or SDAccel open source example on GitHub at https://github.com/Xilinx/SDAccel_Examples. Lastly, this release also introduces the Application Optimization Assistant, allowing users to more efficiently understand and optimize code for the application, not just kernel or host, independently.

- **Performance**
  - Automatic kernel clock scaling allows execution of kernels in hardware without timing closure constraints. In the 2016.2 release, clock scaling is enhanced to be finer grained from 20Mhz to 10Mhz
  - Support for kernel clock frequency increased up to 250Mhz for supported DSAs.
  - Capability to override kernel clock frequency in DSA.

    Note: *The maximum clock frequency should be less than 300 MHz.*
  - Automatic memory coalescing to achieve maximum memory throughput without required code refactoring.
  - Automatic loop pipelining and unrolling allows kernels to achieve higher data throughput without requiring attributes or pragmas. Users can also turn off automatic loop pipelining by setting the enableAutoPipelining flag as shown below:
    - For xocc: `xp param:compiler.enableAutoPipelining=false`
    - For Tcl: `set_param compiler.enableAutoPipelining true`
  - Support for DSA with 2 DDR memory doubles kernel to global memory bandwidth.
  - Examples showing how to improve application memory throughput from host to global and kernel to global memory.
  - Coding templates and examples with supported attributes and techniques for improving kernel performance.

- **Usability**
  - SDAccel installation: `settings64.sh` has been enhanced to set up all the necessary environment variables for executing emulation in command line mode.
  - Enhanced Kernel profiling identifies when kernel performance stalls due to delays in data because of memory inefficiencies.
  - Application Optimization Assistant provides Profile Rule Checks, which is integrated with the Profile Summary Viewer and enables users to focus on the key areas of their kernel. PRCs highlight certain profile results, inform users known issues, and provide improvement recommendations. PRCs work for both hardware emulation and system runs on the FPGA.
  - Streamlined Xilinx Board Installation with new command line utility: xbinst.
  - xocc: Command line compiler similar to gcc for the creation of FPGA programming binaries.
    - Allows parallel compilation of kernels using all cores on the developer workstation.
    - Allows parallel compilation of kernels using lsf cluster job dispatch.
    - Link stage allows users to customize mix of kernels in FPGA programming binary.
    - Link stage enables the insertion of RTL based kernels in a Makefile based environment.
    - Xilinx command line compiler (xocc) also has a simple mode where compile and link stages are combined into a single command sequence as is the case with gcc.
  - Debug support
    - Integrated debug flow using GDB for host code.
    - Ability to set breakpoints in OpenCL kernel code in CPU emulation flow.
    - `printf` support in all development flows: CPU emulation, hardware emulation and while executing kernel in hardware.
  - Host application profiling in all development flows. Profiling report includes API calls, kernel execution, data transfer, top ten kernel execution, top ten buffer writes and top ten buffer reads.
  - Ctrl-C support to terminate applications running on the Alpha Data card
- **Language Support**
  - OpenCL Installable Client Driver (ICD).
  - OpenCL 2.0 pipes support for passing data between kernels.
  - Xilinx OpenCL pipes extension supports blocking read and write for passing data between pipes.
  - OpenCL 2.0 on-chip global memory for passing data between kernels.
  - RTL kernel packaging into xo kernel containers using Vivado®.

- **Device Support Archive (DSA)**
  - Capability to override kernel clock frequency is enabled for all DSAs.

    ***Note**: The maximum clock frequency should be less than 300 MHz.*
  - Automatic kernel clock scaling allows execution of kernels in hardware without timing closure constraints. In 2016.2, clock scaling has been enhanced to be finer grained from 20Mhz to 10Mhz.
  - New *High* Capacity 2DDR DSA v3.0 for Alpha Data ADM-PCIE-KU3 Kintex UltraScale KU60 board (beta).
    - Increased fabric resources for compute units
    - Global memory changes to volatile, between binary loads
  - New 2DDR DSA v3.0 TUL TUL-PCIE-KU115 Kintex UltraScale KU115 board (beta).
    - PCIe Gen3x8, 2DDR
    - Higher density with SmartConnect
  - New 2DDR DSA v3.1 Alpha Data ADM-PCIE-8K5 Kintex UltraScale KU115 board (beta).
    - PCIe Gen3x8, 2DDR
    - Higher density with SmartConnect

- **SDAccel Environment Supported Devices**

Board	Device	Supported DSAs	Kernel Clock Frequency MHz	Status	Features
TUL-PCIE3-KU115	KU115	xilinx:tul-pcie3-ku115:2ddr:3.1	200	Beta	- PCIe Gen3x8, 2 DDR
ADM-PCIE-8K5	KU115	xilinx:adm-pcie-8k5:2ddr:3.1	250	Beta	- PCIe Gen3x8, 2 DDR
ADM-PCIE-KU3	KU60	xilinx:adm-pcie-ku3:2ddr:3.1	250	Production	- PCIe Gen3x8, 2 DDR
ADM-PCIE-KU3	KU60	xilinx:adm-pcie-ku3:2ddr-xpr:3.1	200	Beta	- PCIe Gen3x8, 2 DDR - Increased fabric resources for compute units. Global memory changes to volatile, between binary loads.
ADM-PCIE-7V3	V7690T	xiilinx:adm-pcie-7v3:1ddr:3.0	200	Production	- PCIe Gen3x8, 1DDR

- **Tool and OS Requirements**
  - Vivado Lab Edition 2016.2 for programming the FPGA device on the programming computer.
  - RedHat Enterprise Linux 6.4-6.7, 7.2, or CentOS 6.4-6.7 64-bit.
  - The following packages must be installed on the host machine.
    - $sudo yum install gcc
    - $sudo yum install kernel-devel
    - $sudo yum install glibc.i686 glibc.x86_64

- **Beta Feature**
  - OpenCL runtime supports Power8 architecture for executing OpenCL, C, and C++ applications on FPGA boards compiled with SDAccel.
  - OpenCL runtime has been enhanced to support multiple devices with single host applications.
  - IDE with debug, profiling and application trace view.
    - Eclipse based IDE with support for integrated GDB for debug.
      - Host code debug in all three flows (CPU emulation, Hardware emulation and in hardware)
      - Kernel debug in CPU emulation flow
  - Profiling reports for application optimization in all three flows with increased information and accuracy from CPU emulation to execution on hardware.
  - Application timeline trace provides a holistic view of memory transfers between the host and the device as well as between kernel compute units and device global memory.
    - Enables you to quickly pinpoint data transfer bottlenecks and discover inefficient memory access patterns.
    - Enables you to analyze the impact of concurrent operation of multiple compute units on system performance.
  - Half precision floating-point data type support.
  - DSA creation through Vivado® IP Integrator.
  - Kernels defined from RTL sources in the SDAccel script based mode. This capability is not available in the GUI based flow.

- **Support and Documentation**
  - SDAccel user Forums: https://forums.xilinx.com/t5/SDAccel/bd-p/SDx
  - SDAccel Documentation: http://www.xilinx.com/support/documentation-navigation/development-tools/software-development/sdaccel.html
  - SDAccel Open Source Examples: https://github.com/Xilinx/SDx/tree/master/Examples/SDAccel
  - FAQ and Known issues: https://forums.xilinx.com/t5/SDAccel/FAQ-and-Information/td-p/678389
- **Fixed Known Issues from Previous Release**
  - Issue fixed when `xclbin` was being generated for hold timing violations for some system clocks. Starting with the 2016.2 release, this issue will result in a build failure.
  - SDAccel installation: Setup script now adds all High Level Synthesis (HLS) simulation libraries.
- **Known Issues**
  - Device Support Archive (DSA) Known Issues
    - Maximum number of compute units is limited to 10.
    - In certain cases, the Alpha Data ADM-PCIE-7V3 and ADM-PCIE-KU3 FPGA card may not link up in the PCIe Gen3x8 configuration. This is due to a known errata regarding Avago Technologies ExpressLane™ PEX 8747 (rev CA) PLX technology Gen 3 PCIe switch. The errata of PEX 8747 (rev CA) links up with Xilinx PCIe endpoint as Gen1 x8 instead of Gen3 x8. An eeprom upgrade is required for the PLX switch which customers should be able to obtain directly from Avago Technologies. A Confidential Disclosure Agreement (CDA) may need to be signed for obtaining the patch.
  - OpenCL Compiler Known Issues
    - A `struct` type argument of kernel function cannot contain vector or array type member field.
  - Emulation Flow Known Issues
    - Emulation fails with symbol lookup error:
      `./shared0: undefined symbol: _Z13native_divideff for CPP applications`

      Solution: Wrap the entire top function with extern “C” {...}

Availability

To learn more about the SDAccel development environment, visit www.xilinx.com/sdaccel where you will find QuickTake video tutorials, documentation and links to the SDAccel Development Environment-qualified Alliance members. To access the capabilities of the SDAccel Development Environment, please contact your local sales representative.