FPGA-based Accelerated Cloud Computing with AWS-F1, SDAccel and the CAOS Framework

ICCD 2017 Boston, November 5

https://www.iccd-conf.com/Program_2017.html

Register for the tutorial at:

https://www.xilinx.com/support/university/workshops/schedule.html

The increasing computational requirements of next-generation Cloud and High-Performance Computing (HPC) applications are pushing the adoption of accelerated computing based on heterogeneous architectures into mainstream, as traditional CPU technology is unable to keep pace. FPGA accelerators compliment CPU-based architectures and deliver significant performance and power efficiency improvements.

In this regard, Xilinx FPGAs are now available on the Amazon Elastic Compute Cloud (EC2) F1 instances, which are designed to accelerate data center workloads, including machine learning inference, data analytics, video processing, and genomics. These are available in two different sizes that include up to eight Virtex® UltraScale+ VU9P FPGAs with a combined peak compute capability over 170 TOP/sec (INT8). Furthermore, Amazon Web Services offers the SDAccel™ Development Environment for cloud acceleration, enabling the user to easily and productively develop accelerated algorithms and then efficiently implement and deploy them onto the heterogeneous CPU-FPGA system.

SDAccel completely automates the step of the hardware design flow, offering an easy to use environment for FPGA application design. It offers the possibility to specify a compute kernel using hardware description languages for RTL designs, or C and C++ for higher-level algorithmic implementation, while using OpenCL APIs to control run-time behavior. The high performance and high-level of scalability offered by F1 instances, paired with the power and ease of use of Xilinx SDAccel is very appealing for the development of high high-performance FPGA-based accelerated solutions, and will be the focus of this workshop.

In order to provide an even easier approach to FPGA programming, Politecnico di Milano is developing the CAOS, a CAD framework that helps researchers and practitioners in approaching High Performance Computing (HPC) systems based on FPGA through a semi-automatic workflow that integrates with the SDAccel toolchain. The framework is capable of analyzing the user application and profile it against a set of datasets in order to find the most compute intensive functions. The retrieved information is used to check the applicability of different architectural templates that can augment the application performance. This operation lightens the user's effort from the hardware-software co-design activity. Furthermore, the functions that can be implemented in hardware are automatically optimized through different techniques and the final system is provided to the user ready to be used. Finally, the framework is designed to be capable of integrating modules from different developers in order to stimulate external contributions and open research.

#SDAccelCAOSTutorial

TUTORIAL PROGRAM

- **Introduction to SDAccel, Amazon F1 Instances and CAOS**
- 15m break
- **Tools demonstration**
  - Introduction to the proposed algorithm to accelerate
  - How to design using SDAccel with the GUI flow
  - How to design using SDAccel with the Makefile flow
  - How to design using CAOS
  - How to deploy an AWS EC2 F1 instance
- 15m break
- **Hands-on SDAccel and CAOS**
  - The user will be provided with a non-optimized version of an application and will spend these two hours optimizing it for an Amazon F1 instance using one of the presented approaches.

In order to follow the tutorial, the attendees are required to bring their personal laptop.

ORGANIZERS AND SPEAKERS

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