Dear Educator,

Be the first to get hands-on with a non-obfuscated fully-verified MIPS core for teaching and projects!

The Imagination University Programme is pleased to host two one-day workshops specifically for teachers, based on the soon-to-be released "MIPSfpga" core.
MIPSfpga is a configuration of the MIPS microAptiv family found in many embedded devices, including the popular PIC32MZ microcontroller from Microchip.
This workshop will show you how to use this core as part of a Computer Architecture course, which will pave the way for your students to use this core in their projects, in effect creating their own SoC designs.
With its long heritage and excellent documentation MIPS is the preferred choice of RISC architecture for many teachers around the world. But to demonstrate key concepts in the past; teachers had to settle for creating partial "MIPS-like" cores or using unofficial copies of dubious heritage. Not now! MIPSfpga is the real "industrial" RTL, non-obfuscated, and available freely for academic use.
These workshops are the first in a global programme of events to enable teachers to harness this wonderful technology. You can be among the first to access MIPSfpga!

Teaching Computer Architecture using MIPSfpga and the Xilinx-Digilent Nexys 4 DDR platform

TRAINERS:

- Prof. Sarah Harris, University of Nevada at Las Vegas. Co-Author of "Digital Design & Computer Architecture" by Harris & Harris
- Dr. Parimal Patel, Principal Trainer and Content Developer for the Xilinx University Program ("XUP")
- Munir Hasan & Sachin Sundar, Solutions Engineers at Imagination Technologies

WORKSHOP CONTENT:

- Welcome & Introduction to the Imagination University Programme (“IUP”)
- Introduction to MIPSfpga
- Software Installations: Codescape MIPS SDK & Vivado
    1. Simulation: Increment LEDs program
    2. Nexys4-DDR board: Increment LEDs delay program
    3. Nexys4-DDR board: Synthesizing core
    4. Codescape MIPS SDK: using Codescape to develop & debug C and assembly code
       Bus Blaster/OpenOCD: using the Bus Blaster JTAG probe and OpenOCD to debug a target system
- Lab 1: Writing C code – reaction timer
- Lab 2: Adding 7-segment display I/O and modifying memory amounts
- Integrating Xilinx IP blocks with MIPSfpga
- Porting to other boards – Example: Basys3
- Teaching Materials in Development for MIPSfpga / Wrap-up / Q&A

After your day of training you will be proficient in porting MIPSfpga to a suitable platform, and aware of its potential to revolutionise your teaching of Computer Architecture.
All delegates will be given access to the MIPSfpga core, the full Getting Started Guide (written by Sarah Harris with contributions from Parimal Patel), detailed reference documentation about MIPS microAptiv, and other vital information/programs that enable the whole package to work effectively.
In addition, we plan to make videos of the lectures available online.

FIND OUT ABOUT THE IMAGINATION UNIVERSITY PROGRAMME

Robert Owen and colleagues from Imagination Technologies will be on-hand and available to discuss your interests.

BOOKINGS

These workshops are free of charge for members of academia but places are limited and demand will be strong, so please apply for your place quickly. (However, please do not apply if you are not sure you can attend.)

ELIGIBILITY

- These workshops are open to academic faculty members, with a priority for those involved directly in teaching
- It is unlikely that we will accept more than two delegates from any particular department or group

- We reserve the right to accept or refuse registrations based on our desire to enable the broadest spectrum of Universities and Colleges to participate
- Prior experience of Vivado or Codescape MIPS SDK is useful, but not essential

DATE: Wednesday 13th or Thursday 14th May, 8:30AM to 5PM

VENUE: Harvey Mudd College, Claremont, Southern California, USA

NEARBY ACCOMODATION: The Claremont Doubletree Hotel

PREPARATION: To participate in these hands-on exercises, attendees will need to bring a Windows laptop. Installing Xilinx Vivado (free Webpack Edition) and Imagination's Codescape MIPS SDK (free online edition) in advance will save time on the day.

REGISTRATION: Please apply online here

INFORMATION: To keep in touch about the release of MIPSfpga, please register for the Imagination University Programme here

You are welcome to ***circulate*** this e-mail to academic friends and colleagues…

Our sincere thank you for your interest - we look forward to seeing you in Claremont!

Best Regards,

Manager: Worldwide University Programme
Imagination Technologies
e-mail: Robert.Owen@imgtec.com
Web: http://community.imgtec.com/university/

University Community