ONE DAY WORKSHOPS

Get hands-on with a non-obfuscated fully-verified MIPS core for teaching and projects!

Monday 2nd May, 2016 at Imagination Technologies, Santa Clara
(venue may change to Foothill College, Los Altos Hills)

Wednesday 4th May, 2016 at Portland State University

Imagination University Programme is pleased to host two more workshops specifically for teachers, based on the award winning "MIPSfpga" core. MIPSfpga is the RTL source code of the MIPS microAptiv for implementation on an FPGA. It is a member of the same family found in many embedded devices, including the popular PIC32MZ microcontroller from Microchip, Mediatek/SEEED Studio's new LinkItSmart7688 and Samsung's Artik1.

This workshop will show you how to use this core as part of a Computer Architecture course, which will pave the way for your students to use it in their projects, in effect creating their own SoC designs. MIPSfpga is the real "industrial" RTL, non-obfuscated, and available freely for academic use. These workshops are part of a global programme of events to enable teachers to harness this wonderful technology. You can be among the first to get hands-on with MIPSfpga!

WORKSHOP: Teaching Computer Architecture using MIPSfpga and the Digilent Nexys 4 DDR platform with a Xilinx Artix 7 FPGA

Location & Date

Imagination Technologies Office, Santa Clara: Monday 2nd May, 2016.
(NOTE: we may switch the venue to Foothill College to access a ready-equipped Lab. TBC)

Portland State University, Portland: Wednesday 4th May, 2016.

Agenda

The workshop starts at 09:00 and ends at 17:30

- Welcome & Introduction to the Imagination University Programme (IUP)
- Introduction to MIPSfpga
- MIPSfpga and Vivado Demonstration:
    - Simulation: Increment LEDs program
    - Increment LEDs delay program on the Nexys 4 DDR
    - Synthesizing core on the Nexys4 DDR
    - Codescape MIPS SDK: using Codescape to develop & debug C and assembly code

    - Bus Blaster/OpenOCD: using the Bus Blaster JTAG probe and OpenOCD to debug a target system
- Lab 1: Writing C code
- Lab 2: Adding a 7-segment display I/O
- Integrating Xilinx IP blocks with MIPSfpga
- Porting to other boards – Example: Digilent's Basys3
- Teaching Materials for MIPSfpga / Q&A

After your day of training you will be proficient in porting MIPSfpga to a suitable platform, and aware of its potential to revolutionise your teaching of Computer Architecture.
All delegates will be given access to

- **The MIPSfpga core**
- **The full Getting Started Guide** (written by Prof. Sarah Harris, co-author of Digital Design & Computer Architecture by Harris & Harris, with contributions from Xilinx)
- **Detailed reference documentation** about MIPS microAptiv.
- Other vital information/programs that enable the whole package to work effectively.

Trainers

- Sachin Sundar, Solutions Engineer at Imagination Technologies
- Yuri Panchul, Senior Hardware Design Engineer at Imagination Technologies
- Alex Wong, Technical Systems Analyst & International Sales Manager, Digilent Inc.

Eligibility

- Free of charge for members of academia.
- Open to academic faculty members, with a priority for those involved directly in teaching.
- The workshop will be given in English
- Prior experiences of Vivado or Codescape MIPS SDK are useful but not essential.
- If over-booked, we reserve the right to accept or refuse registrations based on our desire to enable the widest number of universities and colleges to participate.

Registration

Please apply online at here

Find out about the Imagination University Programme

For more information or enquiries, please visit our IUP page or the University Forum .
To stay in touch, please register for the Imagination University Programme here
You are invited to please *circulate* this e-mail to academic friends and colleagues…