**Partial Reconfiguration Flow using Vivado Workshop**

**ZYBO**

**COURSE DESCRIPTION**

The workshop provides professors with an introduction to the partial reconfiguration design flow in Xilinx FPGAs using Vivado Design tools. It covers basic terminologies used in partial reconfiguration technology, provides understanding of the fundamental steps involved in developing a design capable of partial reconfiguration. You will learn the capabilities of and restrictions imposed by the reconfiguration tools. Xilinx Vivado design tools are used for the hardware design and Software Development Kit (SDK) is used for the software development. The current flow is Tcl commands based to develop partial reconfiguration capable designs. Vivado IDE and IP Integrator are used to create initial static design.

# Install Xilinx software

Professors may submit the online donation request form at <http://www.xilinx.com/member/xup/donation/request.htm> to obtain the latest Xilinx software. The workshop was tested on a PC running Microsoft Windows 7 professional edition.

* Vivado 2014.3.1 System Edition with SDK

1. **Setup hardware**

Connect ZYBO

* 1. Set the power supply jumper to USB so the board can be powered up and laboratory assignments can be carried out using single micro-usb cable
  2. Connect micro USB cable between PROG UART port of ZYBO and PC

You will also need a SD card writer.

1. **Install distribution**

Extract the **labsource.zip** file in the *c:\xup\PR* directory. This will create a **labs** folder. The **labdocs\_pdf.zip** file consists of lab documents in the PDF format. Extract this zip file in *c:\xup\PR* directory or any other directory of your choice.

Download the **ZYBO.zip** file and extract it in the **<Vivado\_2014\_3\_install\_dir>\Vivado\2014.3\data\boards\board\_parts\zynq.** This directory is the board files directory and having it in the specified directory will allow you to select Zybo board during the design creation.

1. **For Professors only**

Download the **docs\_source.zip** file using your membership account. Do not distribute them to students or post them on a web site. The **docs\_source.zip** file contains lab documents in Microsoft Word and presentations in PowerPoint format for you to use in your classroom. Note: labsolution.zip is not available due to its size.

1. **Get Started**

Review the presentation slides and step through the lab exercises to complete the labs.

# COURSE AGENDA

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| **Day 1 Agenda** | **Day 1 Materials** |
| Class Intro | 01\_class\_intro.pptx |
| PR Intro | 11\_PR\_Intro.ppt x |
| Vivado Design Flow | 12\_Vivado\_Design\_Flow.pptx |
| Lab 1: Building a Complete Embedded System | 12a\_lab1\_intro.pptx  Lab01.docx |
| PR Design Considerations | 13\_PR\_Design\_Considerations.pptx |
| Partial Reconfiguration Controller | 14\_PRC\_Intro.pptx |
| Debugging PR Design using Vivado Analyzer Cores | 15\_Debugging\_PR\_Design.pptx |
| Lab 2: Using PRC for Hardware Trigger and Debug Lab | 15a\_lab2\_intro.pptx  Lab02.docx |
| IP Integrator and Embedded System Design | 16\_IPI\_And\_Embedded\_System\_Design.pptx |
| **Day 2 Agenda** | **Day 2 Materials** |
| Lab 3: Reconfiguring Processor Peripheral | 16a\_lab3\_intro.pptx  Lab03.docx |
| AXI HWICAP | 17\_AXI\_HWICAP.pptx |
| Lab 4: Reconfiguring Using AXI HWICAP | 17a\_Lab4\_Intro.pptx  Lab04.docx |
| Driving ICAP Resource | 18\_ICAP\_Processor.pptx |
| Lab 5: Reconfiguring Using Custom ICAP Processor | 18a\_Lab5\_Intro.pptx  Lab05.docx |
| Software Triggers in the PRC | 19\_PRC\_SW\_Triggers.pptx |
| Lab 6: Reconfiguring with HW-SW Triggers using the PRC | 19a\_Lab6\_Intro.pptx  Lab06.docx |

**LAB** **DESCRIPTIONS**

Lab 1 - Use Vivado with Partial Reconfiguration (PR) capability enabled to synthesize HDL models and implement the design.

Lab 2 - Use the Partial Reconfiguration Controller (PRC) core to reconfigure a design that has one RP having two RMs. Use the Vivado logic analyzer cores to debug the design.

Lab 3 - Use Vivado IPI and Software Development Kit to create a reconfigurable peripheral using ARM Cortex-A9 processor system on Zynq.

Lab 4 – Use an AXI HWICAP IP to create a reconfigurable design.

Lab 5 – Use the provided light-weight custom IP to access the ICAP resource to reconfigure the design.

Lab 6 - Use the Partial Reconfiguration Controller (PRC) core to reconfigure a design through both hardware and software triggers.

1. **Contact XUP**

Send an email to [xup@xilinx.com](mailto:xup@xilinx.com) for questions or comments