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Emulating External SERDES Devices with Embedded RocketIO Transceivers

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The Virtex-II Pro™ Platform FPGA provides an attractive single-chip solution to serial transceiver design problems that previously required multiple devices. This white paper describes several different dedicated external SERDES devices and presents alternative design solutions using the Virtex-II Pro Platform FPGA with RocketIO™ transceivers.

The four external devices discussed here are the Vitesse™ single-channel VSC7123, the Vitesse quad-channel VSC7216-01, the Texas Instruments™ TLK3101, and the Mindspeed™ CX27201. The features offered by each of these devices are presented, along with a discussion of how the RocketIO transceiver can afford an alternative to each multi-chip solution. Links to Xilinx information resources for the Virtex-II Pro Platform FPGA and embedded RocketIO transceiver are presented in the final section.

Summary

As data transfer speeds have increased, high-speed differential serial lines have replaced large parallel buses in many designs. A Serializer/Deserializer (SERDES) converts parallel data into differential serial data, and differential serial data into parallel data.

The interfacing requirements between a parallel data bus and a SERDES IC on a printed circuit board are implemented by a *Protocol Controller* device (see Figure 1). To increase serial transmission speed, these parallel buses must increase either in width or in data speed. This becomes a troublesome task for the designer when signal integrity and routability issues grow increasingly difficult to resolve.

The Virtex-II Pro Platform FPGA comes with 4, 8, 12, 16, or 20 full-duplex 3.125 Gb/s RocketIO serial transceivers (see Table 1), allowing the designer to integrate the Protocol Controller and SERDES into one device.

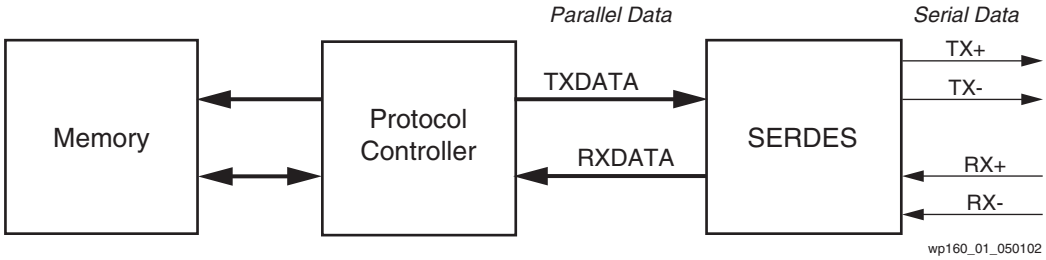

Figure 1: **Data Flow Concept**

Table 1: **Number of Transceivers per Device**

Device	RocketIO Transceivers
XC2VP2	4
XC2VP4	4
XC2VP7	8
XC2VP20	8
XC2VP30	8
XC2VP40	12
XC2VP50	16
XC2VP70	20
XC2VP100	20

Serial Data Transmission Basics

In the transmission of data shown in Figure 1, transceivers send and receive *packets* of data on the serial data lines. Figure 2 shows a simple packet format. Start of Packet (SOP) and End of Packet (EOP) control characters signal the beginning and end of the data to be sent. The Header holds protocol-specific information about the packet, including its source and destination. The Payload is the actual data content being transmitted and received. The Cyclic Redundancy Check (CRC) is a polynomial that is calculated by the transmitter and checked by the receiver. The CRC field is used to determine if an error occurred during data transmission. The protocol controller creates or "frames" these packets, which are then sent to the SERDES for

transmission. The protocol controller also "deframes" received packets, and passes the data on to the data processing logic or memory.

On the data processing side of the controller, data is typically 8 bits wide. It is converted to a 10-bit form for serial transmission, and is converted back to the 8-bit form on the receive side. This conversion is widely known as *8B/10B Encode/Decode*. This 8B/10B encoding allows for DC balancing on the serial line, and creates transitions close enough together in the serial bitstream to support clock extraction and correction.

The implementation comparisons which follow use this packet concept to differentiate sections of the total solution. The protocol controller is called *user logic* in the examples following.

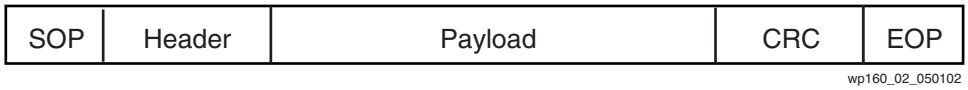

Figure 2: **Packet Format**

Transceiver Design Comparisons

The transceivers in this group are all designed to be used with Ethernet and/or FibreChannel.

The data path models used to describe serial transceivers contain several "layers," as shown in Figure 3. The *physical layer* is often contained in the SERDES, while everything above the GMII comprises the *user logic*.

This white paper focuses on the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) portions of the physical layer. Above the GMII, all needed functionality can be implemented in the FPGA fabric. Below the PCS/PMA layers, the Physical Medium Dependant (PMD) layer can be regarded as common to all the designs discussed here, and is beyond the scope of this paper.

The four discrete SERDES devices and the Virtex-II Pro FPGA embedded RocketIO transceiver each implement the physical layers differently:

- The Vitesse VSC7123 is a single-channel device with a 10-bit parallel data interface. This device implements only the PMA layer; a separate PCS is needed to implement the 8B/10B Encoder/Decoder.
- The Vitesse VSC7216-01 is a four-channel device with an 8-bit interface per channel. It implements both the PCS and PMA layers. The four channels can be "channel bonded" together to increase the maximum serial throughput.
- The Texas Instruments TLK3101 is a single channel device with a 16-bit interface. It also implements both the PCS and PMA layers.
- The Mindspeed CX27201 and the RocketIO transceiver both implement the PCS and PMA, along with several selectable data path widths. The RocketIO transceiver, however, has a greater number of data path width and baud rate options than the CX27201.

Table 2 summarizes the capabilities of the Virtex-II Pro FPGA with RocketIO and the four discrete SERDES devices discussed in this paper.

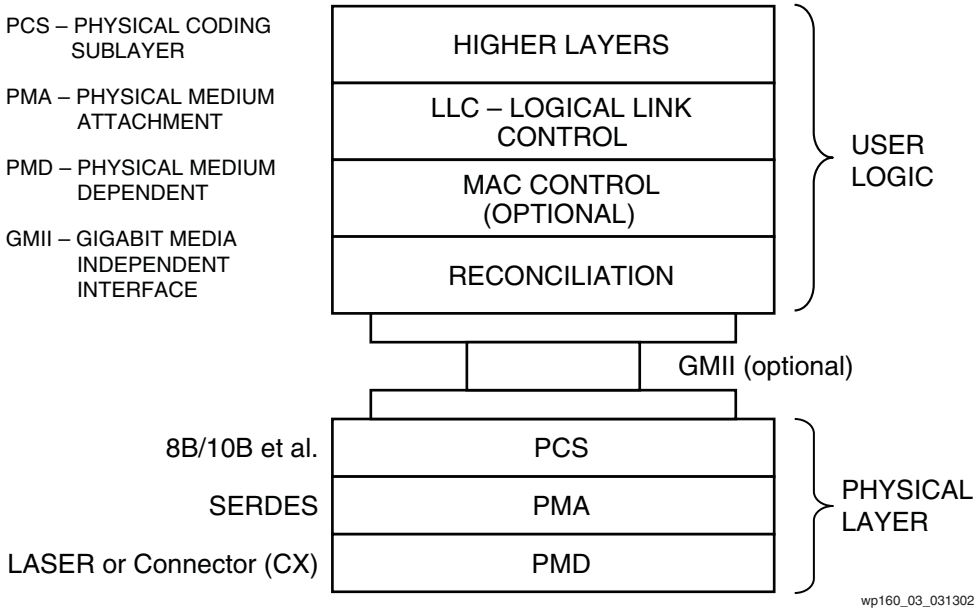

Figure 3: **Serial Data Transfer Layers**

Table 2: **Transceiver Comparison**

Characteristic	Virtex-II Pro FPGA with RocketIO Transceiver	FPGA + Vitesse VSC7123	FPGA + Vitesse VSC7216-01	FPGA + Texas Instruments TLK3101	FPGA + Mindspeed CX27201
Number of Channels	1 to 20(2)	1	4	1	1
Max Baud Rate per Channel	3.125 Gb/s	1.36 Gb/s	1.25 Gb/s	3.125 Gb/s	3.125 Gb/s
Power per Channel at Max Baud Rate	350 mW @ 3.125 Gb/s	650 mW @ 1.36 Gb/s	750 mW @ 1.25 Gb/s	360 mW @ 3.125 Gb/s	650 mW @ 3.125 Gb/s
Max Data Throughput(1)	100 Gb/s(3)	2 Gb/s	8 Gb/s	5 Gb/s	5 Gb/s
User Interface I/Os	4(4)	27	111	41	22 to 46
Halfrate Capable	YES	NO	YES	NO	YES
8B/10B Encoder/Decoder	YES	NO	YES	YES	YES
CRC Capability	YES(5)	NO	NO	NO	NO
Differential Swing Control	YES	NO	NO	NO	YES
Loopback Mode	YES	YES	YES	YES	YES
Footprint Space	1 chip	2 chips	2 chips	2 chips	2 chips

Notes:

1. Approximate full-duplex real data transfer capacity, exclusive of protocol overhead.
2. Depending on Virtex-II Pro device type. See Table 1. Refer to the *Virtex-II Pro FPGA Data Sheet* or *RocketIO Transceiver User Guide* for further details.
3. Refers to Virtex-II Pro XC2VP100 device, containing 20 RocketIO transceivers.
4. Per channel, plus a reference clock I/O (REFCLK) which can be shared among all transceivers using the same reference clock.
5. Single-channel CRC. Most channel-bonded (byte-striped) implementations, as well as single-channel and multi-channel implementations of the Infiniband™ protocol, require CRC computation in the FPGA fabric. Refer to the *RocketIO Transceiver User Guide* for more details.

Vitesse VSC7123

Generic FPGA + VSC7123 Solution

The Vitesse VSC7123 needs another device that implements the PCS—or, more specifically, the 8B/10B encoding. Figure 4 shows what would be needed to complete the entire data flow shown in Figure 4. At the left is the MAC, link layer, and other higher levels that would be implemented in the FPGA fabric, including the PCS (8B/10B encoding/decoding) and CRC creation/comparison logic. The control lines and data would connect to the FPGA I/O and be routed to the VSC7123. These signals consume 24 I/Os from the FPGA, as shown in Figure 4. The required 70 MHz parallel data speed functionality could be very difficult to implement successfully on a PCB.

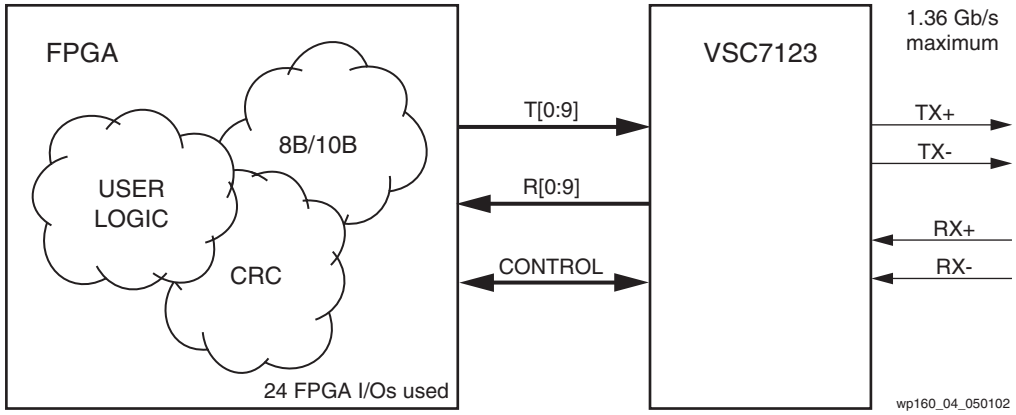

Figure 4: **FPGA + VSC7123 Solution**

Virtex-II Pro FPGA Solution Using Embedded RocketIO Transceiver

The alternative to this solution can be completely integrated into the FPGA logic interfacing to the Virtex-II Pro RocketIO transceiver. This implementation, shown in Figure 5, provides two major advantages. First, the RocketIO transceiver's built-in 8B/10B encoding/decoding function eliminates the need for the FPGA fabric implementation shown in Figure 4. (Alternatively, the designer can use already-designed 8B/10B FPGA logic to connect the 10-bit encoded/decoded data to the RocketIO transceiver, bypassing the RocketIO transceiver's encoding/decoding capability.) Second, containing the control signals (refer to Table 2) inside the FPGA eliminates the need for a large number of external I/O connections.

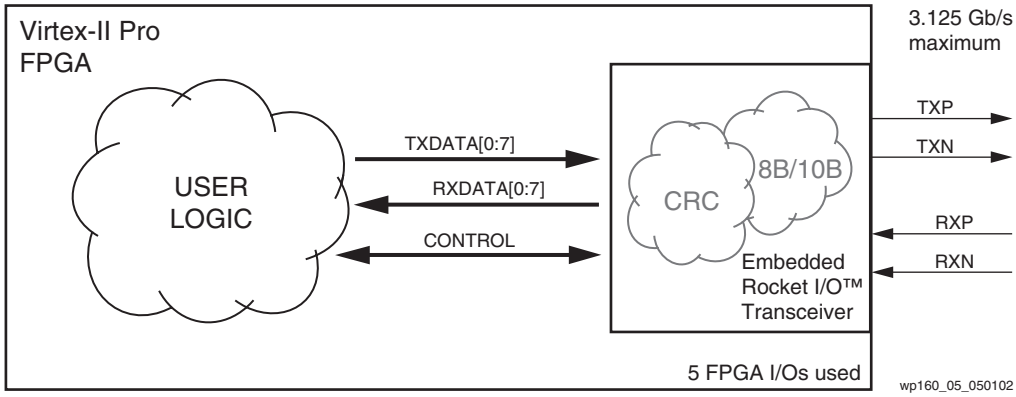

Figure 5: **Virtex-II Pro FPGA Alternative to VSC7123 Solution**

Key advantages include:

- 8B/10B logic doesn't take up FPGA resources—it is part of the transceiver
- Fewer FPGA I/Os used (reduction of 22)
- Less complicated PCB layout
- Signal Integrity issues limited to serial differential I/O signals
- Higher serial baud rates possible than with the VSC7123
- CRC generation and checking is done inside the transceiver (except Infiniband protocol), reducing FPGA logic
- Reduced PCB footprint by integrating the SERDES into the FPGA
- Potential to integrate multiple VSC7123 solutions into a single Virtex-II Pro FPGA
- The RocketIO transceiver retains all of the functionality of the VSC7123

Design Conversion Details

To convert a VSC7123 design to a Virtex-II Pro FPGA solution, the interface can be broken down into three groups:

1. Signals needed to transmit
2. Signals needed to receive
3. Status and control signals

Table 3 shows how the signals between these two transceivers correspond to each other, and which group the signal is associated with. See the *RocketIO Transceiver User Guide* for detailed information.

Table 3: **RocketIO Transceiver / VSC7123 Signal Correlation**

Control	I/O Type	RocketIO Name	External	VSC7123 Name	External
Transmit Data	TX	TXCHARDISPMODE, TXCHARDISPVAL, TXDATA	NO	T[0:9]	YES
Receive Data	RX	RXCHARISK, RXRUNDISP, RXDATA	NO	R[0:9]	YES
Receive Data Is Comma(1)	Ctrl	RXCOMMADET / RXCHARISCOMMA	NO	COMMADET	YES
Enable Comma Detection(2)	Ctrl	MCOMMA_DETECT(5), PCOMMA_DETECT(5)	NO	ENCDET	YES
Data Valid(3)	Ctrl	RXNOTINTABLE	NO	SIGDET	YES
Loopback Enable(4)	Ctrl	LOOPBACK[1:0]	NO	EWRAP	YES
Serial Lines		TXN, TXP, RXN, RXP	YES	TX+, TX-, RX+, RX-	YES

Notes:

1. RXCOMMADET and RXCHARISCOMMA are similar to COMMADET. See the *RocketIO Transceiver User Guide* for details.
2. MCOMMA_DETECT and PCOMMA_DETECT allow if plus and/or minus commas are detected, while ENCDET doesn't. See the *RocketIO Transceiver User Guide* for details.
3. RXNOTINTABLE and SIGDET are equivalent except for polarity. See the *RocketIO Transceiver User Guide* for details.
4. LOOPBACK allows both serial and parallel loopback, while EWRAP allows only serial. See the *RocketIO Transceiver User Guide* for details.
5. Attribute, not a signal.

Vitesse VSC7216-01

Generic FPGA + VSC7216-01 Solution

The Vitesse VSC7216-01 contains four 8-bit interface channels. The PCS is contained inside the device, eliminating one block that was needed for the VSC7123 implementation. Control signals are needed for each separate channel, however. Figure 6 shows the implementation of this device. The maximum serial speed of the channels is 1.25 Gb/s per channel for a combined baud rate of 5 Gb/s per device. This device has over 111 data/control lines that must interact with the user logic on the FPGA. These signals must also run at 50 MHz on the board, which is not a trivial task.

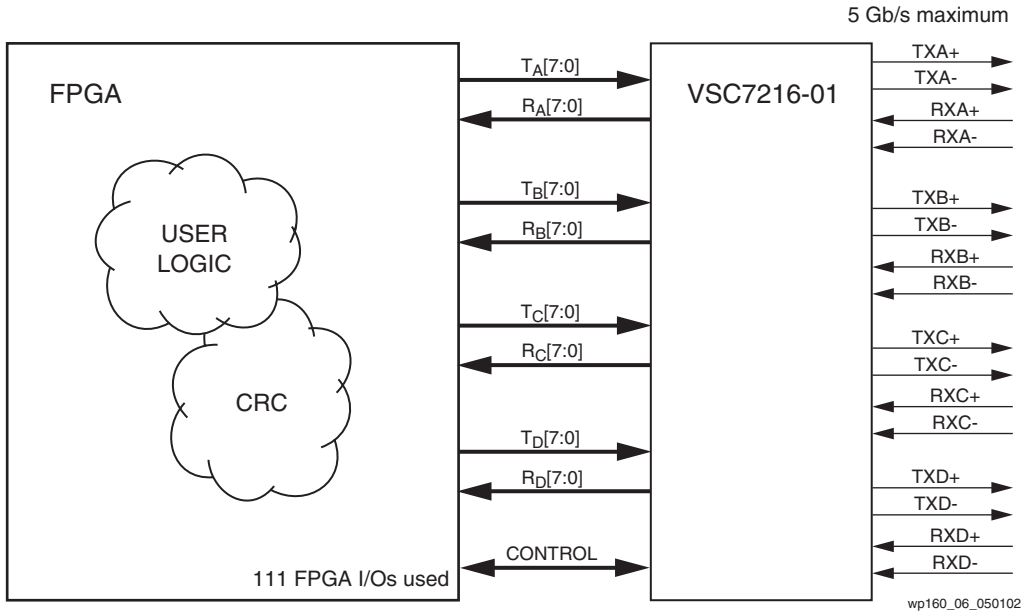

Figure 6: **FPGA + VSC7216-01 Four-Channel Solution**

Virtex-II Pro FPGA Solutions Using Embedded RocketIO Transceivers

The Virtex-II Pro solutions integrate all four VSC7216-01 channels into a single FPGA device (shown in Figure 7 and Figure 8) reducing the number of I/Os to the eight TX+/- and eight RX+/- signals, along with one reference clock. Table 4 shows the control signals corresponding to these two transceivers, including the VSC7216-01's KCHAR signal and the RocketIO transceiver's TXCHARISK, which indicate that the data transmitted is a control character. Although the user interface of the RocketIO transceiver must run at 200 MHz inside the FPGA fabric to obtain the same serial rate as the VSC7216-01, this speed can be accomplished with the Virtex-II Pro FPGA.

The advantages of the Virtex-II Pro solution are:

- Fewer FPGA I/Os used (reduction of 95)
- Less complicated PCB layout
- Signal Integrity issues limited to serial differential I/O signals
- CRC generation/checking done inside the transceiver (Xilinx Aurora and Custom protocols only), reducing use of FPGA logic resources
- Potential to integrate multiple VSC7216-01 solutions into one Virtex-II Pro FPGA
- Reduced PCB footprint by integrating the external SERDES into the FPGA
- Channel Bonding still used for quick porting of user logic, minimal design change
- The RocketIO transceiver retains all of the functionality of the VSC7216-01

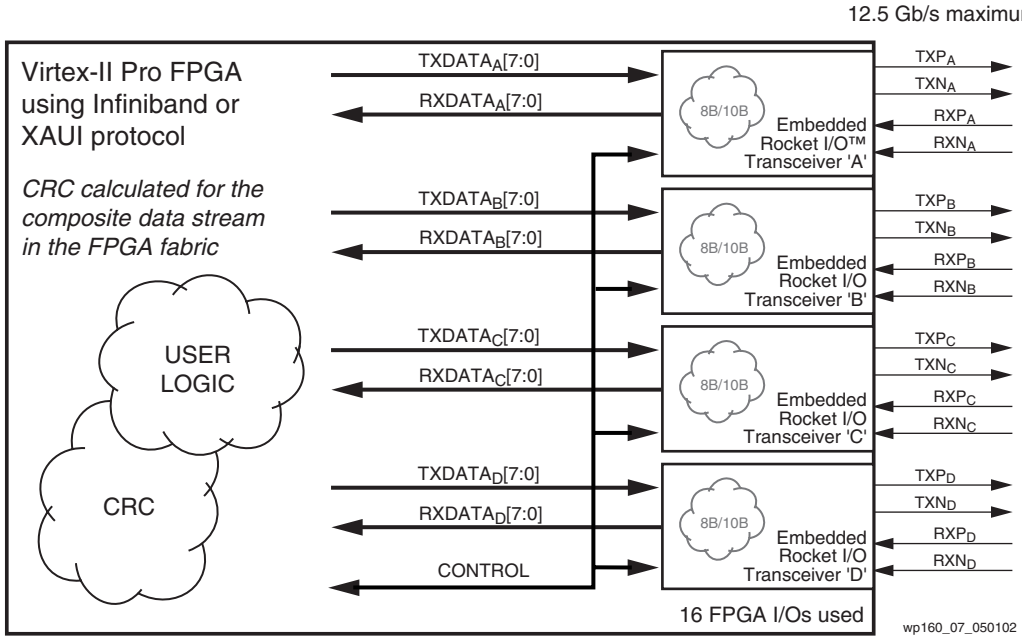

Figure 7: **Virtex-II Pro FPGA 4-Channel Alternative to VSC7216-01 (Infiniband or XAUI)**

Note that the Infiniband and XAUI protocols do not allow byte-striping. Therefore, the CRC must be implemented in the FPGA fabric, as shown in Figure 7 above.

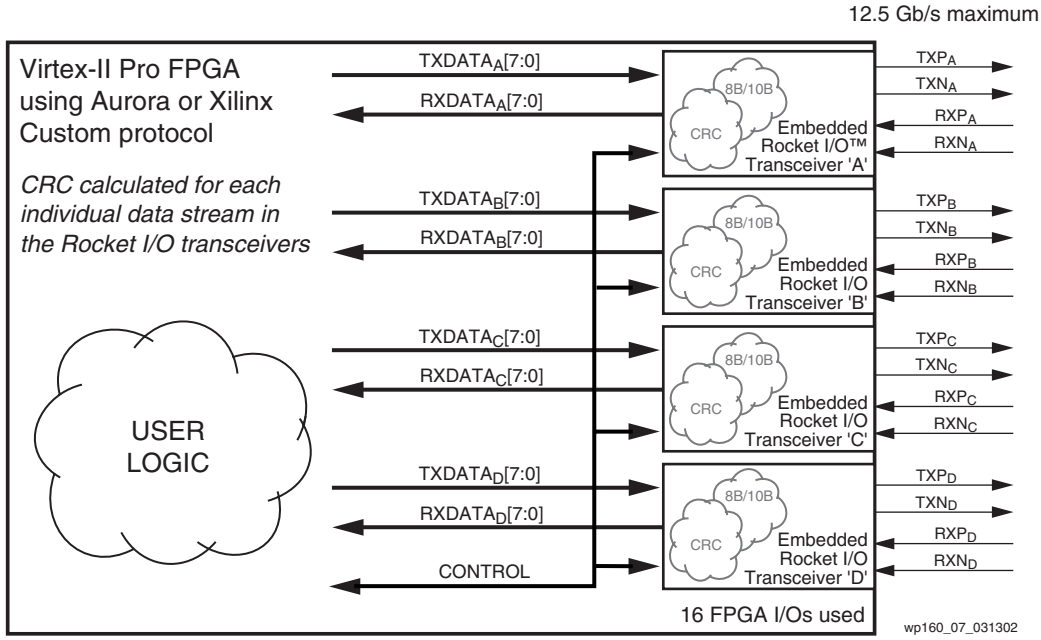

Figure 8: **Virtex-II Pro FPGA 4-Channel Alternative to VSC7216-01 (Aurora, Custom)**

The Xilinx Aurora protocol allows for byte-striping implementation, permitting the RocketIO transceiver's internal CRC capability to be used in multiple-channel configurations, as shown in Figure 8. This frees up FPGA fabric resources for user logic design needs.

Design Conversion Details

To convert a VSC7216-01 design to a Virtex-II Pro FPGA solution, the interface can be broken down into three groups:

1. Signals needed to transmit
2. Signals needed to receive
3. Status and control signals

Table 4 shows how the signals between these two transceivers correspond, and which group the signal is associated with. See the *RocketIO Transceiver User Guide* for details.

Table 4: **RocketIO Transceiver / VSC7216-01 Signal Correlation**

Control	I/O Type	RocketIO Name	External	VSC7216-01 Name	External
Transmit Data	TX	TXDATA	NO	T[7:0]	YES
Receive Data	RX	RXDATA	NO	R[7:0]	YES
Control/Data Character(1)	Ctrl	TXCHARISCOMMA	NO	C/D	YES
Transmit Data Is Control(1)	TX	TXCHARISK	NO	KCHAR	YES
Word Sync Enable(2)	Ctrl	N/A	NO	WSEN	YES
Loopback Enable(1)	Ctrl	LOOPBACK[1:0]	NO	LBEN[1:0]	YES
Detect IDLE(3)	Ctrl	N/A	NO	IDLE	YES
Receive Data Is Control	RX	RXCHARISK	NO	KCH	YES
Receive Error	RX	RXDISPERR / RXNOTINTABLE(4)	NO	ERR	YES
8B/10B Bypass(5)	Ctrl	TXBYPASS8B/10B / RX_DECODE_USE(9)	NO	ENDEC	YES
Data Is a Comma(6)	Ctrl	MCOMMA_DETECT(9), PCOMMA_DETECT(9)	NO	PSDET	YES
Data Is a Comma(6)	Ctrl	MCOMMA_DETECT(9), PCOMMA_DETECT(9)	NO	RSDET	YES
Transmit Buffer Error	Ctrl	TXBUFFERR	NO	TBERR	YES
Half/Full Rate (clock)(7)	Ctrl	SERDES_10B(8,9)	NO	DUAL	YES
Half/Full Rate (data)(7)	Ctrl	SERDES_10B(9)	NO	RATE	YES
Serial Lines		TXN, TXP, RXN, RXP	YES	TX-, TX+, RX-, RX+	YES

Notes:

1. Truth tables are different. See the *RocketIO Transceiver User Guide* for details.
2. WSEN is emulated by setting CHAN_BOND_MODE. See the *RocketIO Transceiver User Guide* for details.
3. The 'Detect IDLE' function can be emulated by a number of different RocketIO signals. The user may review the available signals and their meanings in the *RocketIO Transceiver User Guide*.
4. RXDISPERR / RXNOTINTABLE provide a more descriptive readback of the error that occurred than the Vitesse ERR signal. Several other signals are also used for RocketIO error detection. See the *RocketIO Transceiver User Guide* for details.
5. RocketIO transceivers use a signal and an attribute to emulate the one Vitesse signal.
6. RocketIO transceiver attributes static, Vitesse dynamic.
7. One RocketIO attribute emulates two Vitesse signals.
8. User must change RocketIO transceiver clock inputs manually.
9. Attribute, not a signal.

Using an Alternative 32-Bit Internal Data Interface

The user logic speed is dependant upon the RocketIO transceiver data width. The designer can reduce the parallel data speed requirements of the RocketIO transceiver implementation by using a 32-bit data interface. The advantages of this design (shown in Figure 9) include:

- Reduced logic speed requirements (only 50 MHz)
- Channel Bonding still feasible
- CRC generation/checking done in the transceiver (except Infiniband protocol), reducing use of FPGA logic resources
- The single-channel RocketIO transceiver retains all of the functionality of the four-channel VSC7206-01 implementation, albeit with a moderate serial speed penalty (3.125 Gb/s compared to 5 Gb/s).

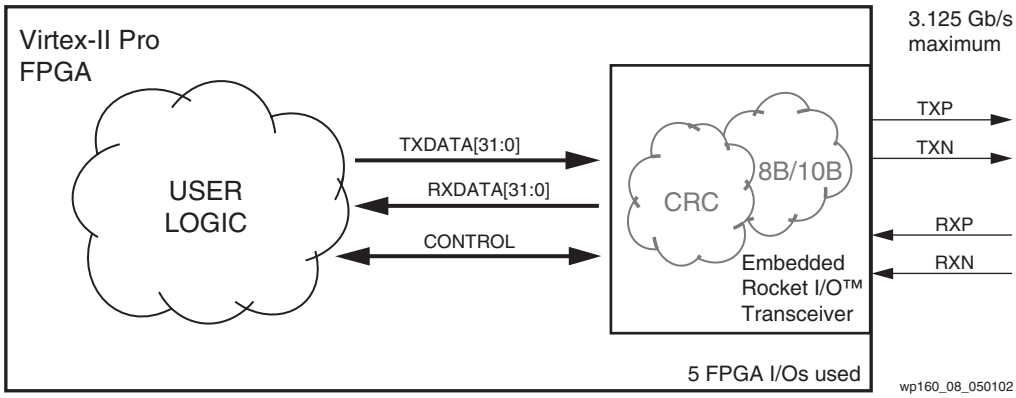

Figure 9: **Virtex-II Pro FPGA 4-Byte Alternative to VSC7216-01**

Texas Instruments TLK3101

Generic FPGA + TLK3101 Solution

The Texas Instruments TLK3101 is one of a five-member family (TLK1501, TLK2501, TLK2701, TLK2711, and TLK3101) of 16-bit-interface, single-channel transceivers. The five members range in maximum serial speed from 1.5 Gb/s (TLK1501) to 3.125 Gb/s (TLK3101). As with the devices discussed previously, the TLK3101 needs a large number of FPGA I/Os to interface to the user logic. A total of 43 signals must be routed on the PCB at high clock rates, though the TLK3101 does improve upon the serial baud rate per parallel signal of the previously discussed devices. Figure 10 shows what would be required for this implementation.

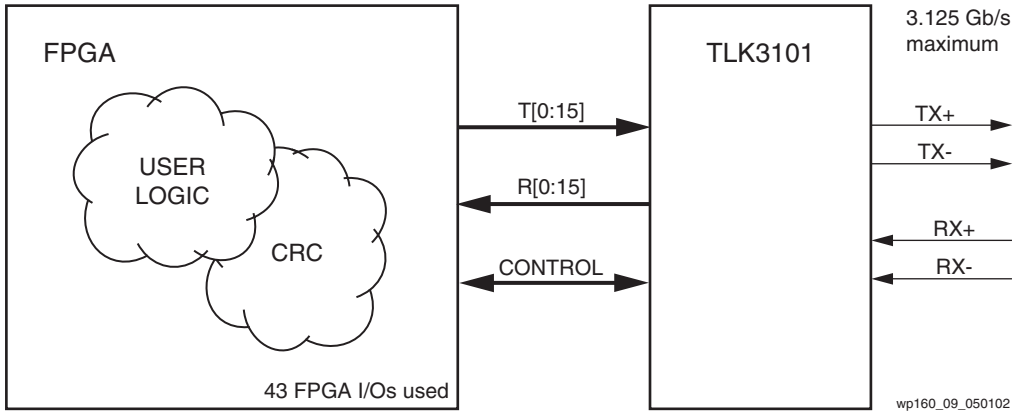

Figure 10: **FPGA + TLK3101 Solution**

Virtex-II Pro FPGA Solution Using Embedded RocketIO Transceiver

The Virtex-II Pro FPGA solution, shown in Figure 11, is an alternative to the TLK3101 design. With its 16-bit parallel interface, the user logic interfacing to the 3.125 Gb/s RocketIO transceiver runs at 156 MHz, a very reasonable speed inside the FPGA fabric. The RocketIO transceiver implementation provides several advantages:

- Reduced PCB footprint by integrating the external SERDES into the FPGA
- Fewer FPGA I/Os used (reduction of 34)
- Less complicated PCB layout
- Signal Integrity issues limited to serial differential I/O signals
- CRC generation/checking done inside the transceiver (except Infiniband protocol), reducing use of FPGA logic resources
- Potential to integrate multiple TLK3101 solutions into a single Virtex-II Pro FPGA
- 32-bit data width can further reduce required speed of user logic (80 MHz)
- Ability to Channel Bond multiple channels
- The RocketIO transceiver retains all of the functionality of the TLK3101

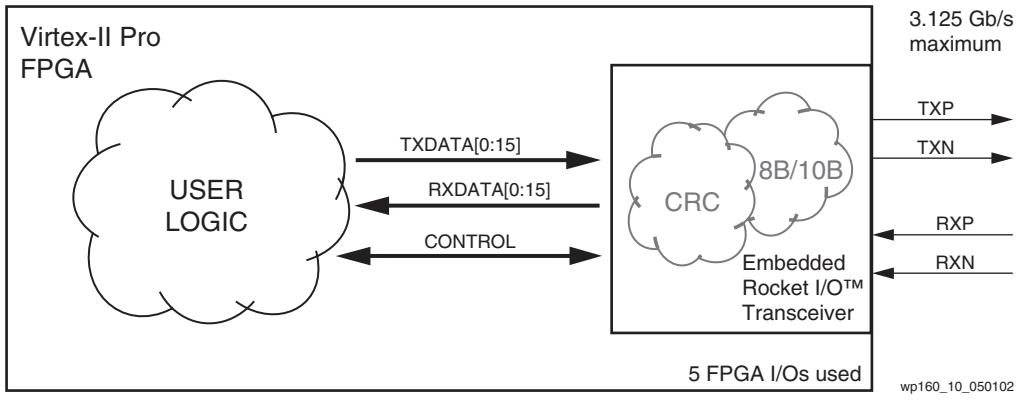

Figure 11: **Virtex-II Pro FPGA Alternative to TLK3101 Solution**

Design Conversion Details

To convert a TLK2501 design to a Virtex-II Pro FPGA solution, the interface can be broken down into three groups:

1. Signals needed to transmit
2. Signals needed to receive
3. Status and control signals

Table 5 shows how the signals between these two transceivers correspond to each other, and which group the signal is associated with. See the *RocketIO Transceiver User Guide* for detailed information.

Table 5: **Virtex-II Pro FPGA / TLK3101 Signal Correlation**

Control	I/O Type	RocketIO Name	External	TLK3101 Name	External
Transmit Data	TX	TXDATA	NO	TXD[7:0]	YES
Receive Data	RX	RXDATA	NO	RXD[7:0]	YES
Loopback Enable(1)	Ctrl	LOOPBACK[1:0]	NO	LOOPEN	YES
Random Bitstream Test(2)	Ctrl	N/A	NO	PRBSEN	YES
Transmit Enable(3)	Ctrl	TXINHIBIT	NO	TX_EN	YES
Transmit Error(3)	Ctrl	TXKERR	NO	TX_ER	YES
Enable Transceiver(3)	Ctrl	POWERDOWN	NO	ENABLE	YES
Receiver Error	Ctrl	RXDISPERR / RXNOTINTABLE(4)	NO	RX_ER/PRBS_PASS	YES
Loss of Signal/Data Valid	Ctrl	RXLOSSOFSYNC	NO	RX_DV/LOS	YES
Serial Lines		TXN,TXP,RXN,RXP	YES	DINRXN, DINRXP, DOUTTXN, DOUTTXP	YES

Notes:

1. LOOPBACK allows both a serial and parallel data path loopback test, while LOOPEN only allows serial. See the *RocketIO Transceiver User Guide* for details.
2. This feature can be emulated in the RocketIO transceiver using LOOPBACK and a simple stream of data.
3. Polarities may be different. See the *RocketIO Transceiver User Guide* for details.
4. Several other signals are also used for error detection. See the *RocketIO Transceiver User Guide* for details.

Mindspeed CX27201

Generic FPGA + CX27201 Solution

The Mindspeed CX27201 is a 1 Gb/s to 3.125 Gb/s SERDES transceiver with bypassable 8B/10B encoding/decoding. Both 8-bit and16-bit data path widths are supported (10-bit or 20-bit widths if the CX27201's 8B/10B capability is bypassed). The CX27201 allows programmability of four levels of differential voltage swing, two selectable termination values, and loopback diagnostic capabilities. A 16-bit implementation is shown Figure 12. As with all external SERDES, the CX27201 uses a large number of FPGA I/Os that must be routed on the PCB.

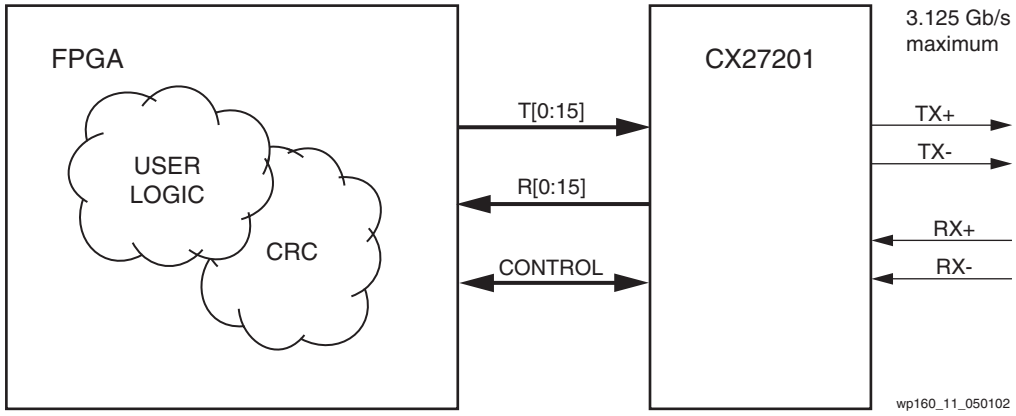

Figure 12: **FPGA + CX27201 Solution**

Virtex-II Pro FPGA Solution Using Embedded RocketIO Transceiver

The Virtex-II Pro FPGA solution is shown in Figure 13.

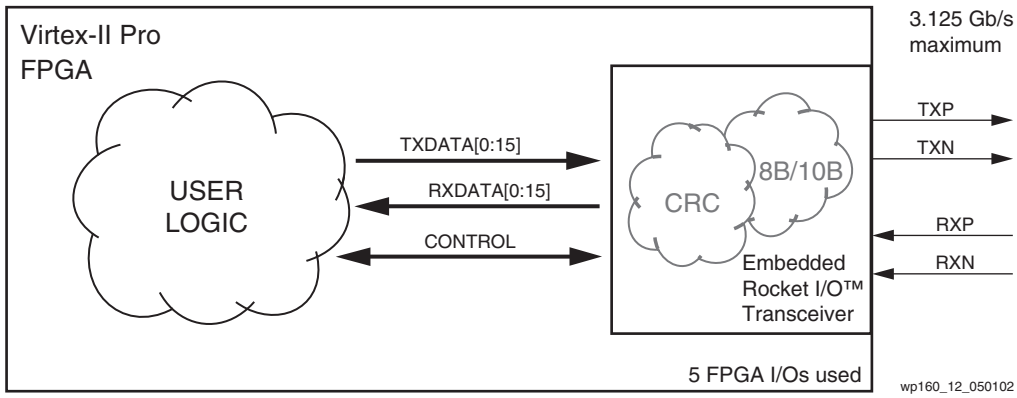

Figure 13: **Virtex-II Pro FPGA Alternative to CX27201 Solution**

The RocketIO transceiver incorporates the same Mindspeed SkyRail™ technology embodied in the CX27201 and supports all its features, including:

- Differential swing control
- Multiple data-width interfaces
- Similar extensive control/status signals
- Available half-rate, providing serial data rates down to 622 Mb/s

In addition, many more features can be implemented using the Xilinx software tools and the FPGA fabric. See the *RocketIO Transceiver User Guide* for an in-depth discussion of these programmable capabilities.

The Virtex-II Pro FPGA solution provides the following advantages:

- Fewer FPGA I/Os used (reduction of up to 41)
- Less complicated PCB layout
- Signal Integrity issues limited to serial differential I/O signals
- CRC generation/checking done inside the transceiver (except Infiniband protocol), reducing use of FPGA logic resources
- Potential to integrate multiple CX27201 solutions into a single Virtex-II Pro FPGA

- Reduced PCB footprint by integrating the external SERDES into the FPGA
- 32-bit data width can further reduce required speed of user logic (80 MHz)
- Ability to Channel Bond up to 16 channels with a single chip
- The RocketIO transceiver retains all of the functionality of the CX27201

Design Conversion Details

To convert a CX27201 design to a Virtex-II Pro FPGA solution, the interface can be broken down into three groups:

1. Signals needed to transmit
2. Signals needed to receive
3. Status and control signals

Table 6 shows how the signals between these two transceivers correspond to each other, and which group the signal is associated with. See the *RocketIO Transceiver User Guide* for detailed information.

Table 6: **Virtex-II Pro FPGA / CX27201 Signal Correlation**

Control	I/O Type	RocketIO Name	External	CX27201 Name	External
Transmit Data	TX	TXDATA	NO	T[7:0]	YES
Receive Data	RX	RXDATA	NO	R[7:0]	YES
Receive Data Is Comma	Ctrl	RXCOMMADET / RXCHARISCOMMA(1)	NO	COMDET	YES
Comma Detect Enable(2)	Ctrl	MCOMMA_DETECT(9), PCOMMA_DETECT(9)	NO	EN_CDET	YES
Receive Data Error Occurred	Ctrl	RXDISPERR / RXNOTINTABLE(8)	NO	RERR[1:0](3)	YES
Loopback Enable(4)	Ctrl	LOOPBACK[1:0]	NO	EWRAP	YES
Transmit Control Character	TX	TXCHARISK	NO	SEND_CM	YES
Analog Preemphasis(5)		TX_PREEMPHASIS(9)	NO	EMP	YES
Serial Differential Voltage	Ctrl	TX_DIFF_CNTRL(9)	NO	SWING	YES
Receive Data Is Control Data	RX	RXCHARISK[1:0]	NO	RKCH[1:0]	YES
8B/10B Bypass	Ctrl	TXBYPASS8B/10B / RX_DECODE_USE(9)	NO	B8TO10_EN	YES
Powers Off Transceiver	Ctrl	POWERDOWN	NO	PW_DOWN	YES

Table 6: **Virtex-II Pro FPGA / CX27201 Signal Correlation *(Continued)***

Control	I/O Type	RocketIO Name	External	CX27201 Name	External
Half/full Rate(7)	Ctrl	SERDES_10B(9)	NO	MODE	YES
Serial Lines		TXN, TXP, RXN, RXP	YES	DINRXN, DINRXP, DOUTTXN, DOUTTXP	YES

Notes:

1. RocketIO transceiver allows two signals with slightly different definitions. See the *RocketIO Transceiver User Guide* for details.
2. RocketIO transceiver allows selection of plus and/or minus comma detection. See the *RocketIO Transceiver User Guide* for details.
3. These two bits indicate the same errors as the RocketIO signals, but the truth table may be different.
4. LOOPBACK allows both serial and parallel loopback, while EWRAP allows only serial. See the *RocketIO Transceiver User Guide* for details.
5. TX_PREEMPHASIS allows for more levels of preemphasis than EMP. See the *RocketIO Transceiver User Guide* for details.
6. RocketIO transceivers use a signal and an attribute to emulate the one CX27201 signal. However, the precise meaning is not exactly equivalent. See the *RocketIO Transceiver User Guide* for details.
7. RocketIO transceiver control is static, CX27201 is dynamic. See the *RocketIO Transceiver User Guide* for details.
8. Several other signals are also used for error detection. See the *RocketIO Transceiver User Guide* for details.
9. Attribute, not a signal.

Cyclic Redundancy Check (CRC)

All the external SERDES solutions discussed in this white paper need user logic to calculate Cyclic Redundancy Check (CRC).

- On Transmit, the user logic must calculate the CRC polynomial for the data packet and send it to the SERDES.
- On Receive, the SERDES receives the polynomial sent by the transmitting terminal while the user logic recalculates the polynomial from the received data. The two polynomials—the received and the recalculated—are then compared and, depending on the results, the user logic decides what action to take. A miscompare of the receive CRC typically results in an error being registered.

Another important advantage of the RocketIO transceiver is that it can compute single-channel CRC on its own (excepting the Infiniband protocol's CRC), eliminating the need for external CRC logic in the FPGA fabric. In multiple-bitstream, channel-bonded designs using the Infiniband or XAUI protocol, CRC computations must be made for the whole composite data stream inside the FPGA fabric and ahead of the channel-bonded RocketIO transceivers, since these protocols do not support byte-striping.

The Xilinx Aurora protocol, however, was designed to allow multi-channel CRCs to be calculated for each discrete RocketIO bitstream, thus eliminating CRC logic from the FPGA fabric in a channel-bonded environment. This same capability is provided to the custom protocol designer using the RocketIO transceiver's Custom mode. These two channel-bonding scenarios are illustrated in Figure 7 (Infiniband and XAUI protocols) and Figure 8 (Xilinx Aurora and Custom protocols).

The RocketIO transceiver also includes the capability to force CRC errors, and has a CRC error detection signal for testing CRC error handling in the user logic. The user logic decides only what action to take; all the other polynomial calculations and comparison are done inside the RocketIO transceiver itself.

Conclusion

The maximum serial data rate and other comparative information for the RocketIO transceiver and various SERDES devices discussed here are shown in Table 2. These five solutions each resolve the physical layers differently:

- The VSC7123 has a 10-bit parallel data interface, and implements only the PMA part of the physical layer. A separate PCS is needed to implement the 8B/10B Encoder/Decoder. Refer to Table 3.
- The VSC7216-01 is a four-channel solution (8-bit interface per channel) that includes both the PCS and PMA. These four channels can be "channel bonded" together to increase the maximum throughput of the serial lines. Refer to Table 4.
- The TLK3101 is a 16-bit interface, single-channel device that also includes the PCS and PMA. Refer to Table 5.
- Both the RocketIO transceiver and the CX27201 SERDES (from which the RocketIO technology was developed) contain the PCS and PMA, and feature multiple selectable data path widths and data rates. The RocketIO transceiver, however, has a greater number of options for data widths and rates than the CX27201. Refer to Table 6.

The Virtex-II Pro FPGA solution with embedded RocketIO transceivers allows the user flexibility in data interface width, logic clock speeds, and overall ease of use. Designer control over the RocketIO solution is also very extensive. The main features include:

- Integration of multiple SERDES devices into the FPGA. The Virtex-II Pro family members contain 4, 8, 12, 16, or 20 transceivers per device.
- CRC generation/checking logic and 8B/10B encoder/decoder are part of the transceiver. No need for extra logic using up FPGA resources. (CRC implementations for Infiniband and for XAUI channel-bonded data streams require FPGA fabric logic.)
- Drastically reduces the number of simultaneous switching outputs from the FPGA.
- Reduces PCB footprint by integrating SERDES and Protocol Controller into one device.
- Allows parallel clock variation by data path width adjustment to reduce clocking speeds that must be met for specific protocols.
- Supports a range of 622 Mb/s to 3.125 Gb/s
- Retains all of the functionality of the external SERDES devices.

All of these advantages allow the Virtex-II Pro RocketIO transceiver to be a viable alternative to an external SERDES.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/30/02	1.0	Initial Xilinx release.
10/22/02	1.1	Updated to include additional Virtex-II Pro family members
07/27/04	1.2	Updated Table 1 and Table 2.