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Spartan-3 vs. Cyclone II Performance Analysis

Cyclone II Performance Drops In Recent Releases

By: Steve Sharp, Xilinx, Inc.

When publishing FPGA device speed models for software (commonly referred to as "speed files"), it is very important to consider the effect on a user of changes that might be necessary to the speed files in the future. If initial speed files are overly pessimistic in the early releases, there may be additional speed in the device that isn't modeled in the speed file, but at least this provides some guard band to help ensure performance.

On the other hand, the opposite case of releasing very aggressive, fast speed files only to find out that they must be degraded or slowed down in the future can be disastrous. If a design met timing by a slight margin in the initial release, a much slower speed file release for the same speed grade could force a customer into a faster, more expensive speed grade just to meet timing or even make it impossible to meet timing at all. The speed change downward can also cause a schedule impact to the design due to the need to modify (perhaps even re-architect) and verify the design.

Xilinx takes a conservative and cautious approach to modeling device speed until sufficient data is available across many devices to ensure the customer will not be adversely impacted by unexpected slow downs in device speed files in the future. We use a combination of simulation and device characterization data with built-in guard bands to ensure we can deliver the reported speed.

Newer Quartus Software Reflects Significantly Slower Timing Numbers for Cyclone II Devices

Cyclone II performance decreased from Quartus II 4.1 to Quartus II 4.2 sp1. The following table shows the combinatorial cell, carry chain and setup and clock to out delays in picoseconds gathered within Quartus using the TCL command *device get_timing* in combination with Quartus *timing analyzer* tool. All through this document, we consider the most cost effective speed grade for both Cyclone II (dash 8) and Spartan™-3 (dash 4) devices.

Timing Arc Changes

As the table below shows, combinatorial delays for the LUT and the carry chain became slower in the later release. The fastest pin delay to the LUT (DATAD) got 2.5 times slower going from Quartus II version 4.1 to 4.2 sp1.

Timing also changed drastically for the setup and the clock to output of the fabric flip-flops.

Table 1: **LUT Delays in Picoseconds**

	Quartus II 4.1	Quartus II 4.2 sp1	Increased Delay %
DATAA – COMBOUT (1)	627	644	2.7
DATAB – COMBOUT (1)	587	616	4.9
DATAC – COMBOUT (1)	262	403	53.8
DATAD – COMBOUT (1)	89	220	147.2

Note:

1. Extracted using *device get_timing* tcl command, e.g., device get_timing cycloneii ep2c5q208c8 lcell_comb dataa combout.

Table 2: **Carry Chain Delays in Picoseconds**

	Quartus II 4.1	Quartus II 4.2 sp1	Increased Delay %
DATAA – COUT (1)	951	610	-35.9
DATAB – COUT (1)	898	580	-35.4
CIN – COMBOUT (1)	60	603	905.0
DATAA-COUT (1)+ CIN-COMBOUT(1)	1011	1213	20.0
CarryChain (CIN-COUT) (2)	60	71	18.3

Notes:

1. Extracted using *device get_timing* tcl command, e.g., device get_timing cycloneii ep2c5q208c8 lcell_comb dataa combout
2. 2. Based on the *timing analyzer*

Table 3: **Fabric Flip-flop Delays in Picoseconds**

	Quartus II 4.1	Quartus II 4.2 sp1	Increased Delay %
Setup (2)	153	-52	-134
Clock Out (2)	162	367	126.5
Setup+Clock Out (2)	315	315	0

Note:

1. Based on the *timing analyzer*

Impact on Design Performance (Comparing Cyclone II Performance on Two Different Versions of Quartus II)

Using a HDL design suite of customer designs, Cyclone II performance was compared between Quartus II versions 4.1 and 4.2 sp1. The netlists used as input for both versions of Quartus II were identical, obtained from Synplify 8.0. All runs including synthesis were timing driven using the highest place and route effort in Quartus.

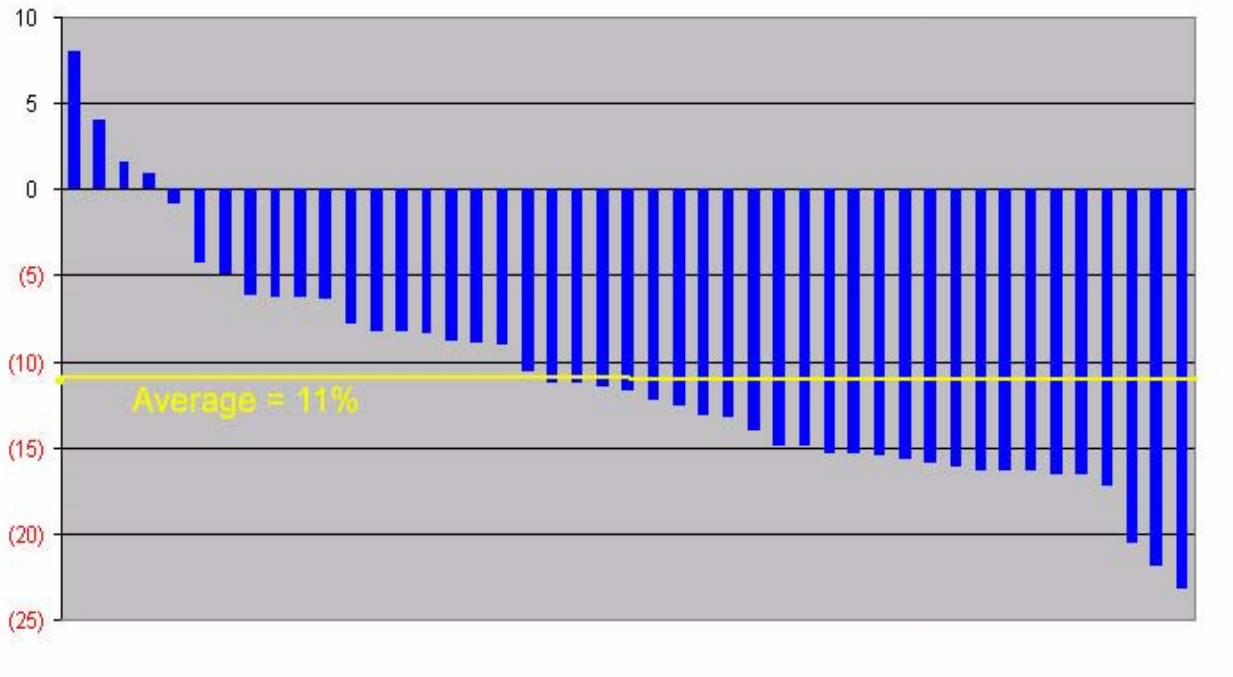

Figure 1: **Cyclone II Percentage Change Going from Quartus II 4.1 to 4.2_sp1**

On average, Cyclone II design performance has slowed down an average of 11%, or almost a full speed grade, from the Quartus II 4.1 release to version 4.2.

Although Quartus II v5.0 has been announced, we have not been able to obtain a full feature copy in order to re-run the benchmark suite using this latest version. We have, however, spot-checked some of the key timing arcs mentioned previously and have found many of them demonstrating slower numbers in v5.0 than in v4.2, so it is expected that the average Cyclone II design performance will fall further in Quartus II 5.0.

Comparing Spartan-3 Performance to Current Cyclone II Performance

With the same customer suite of HDL designs, performance of current Spartan-3 and Cyclone II devices are now compared. Netlists were generated with Synplify Pro 8.0. The highest effort is used in both place and route tools.

The results of these benchmarks show that Spartan-3 designs outperform Cyclone II designs by an average of 3%. The following figure shows all of the results for this test.

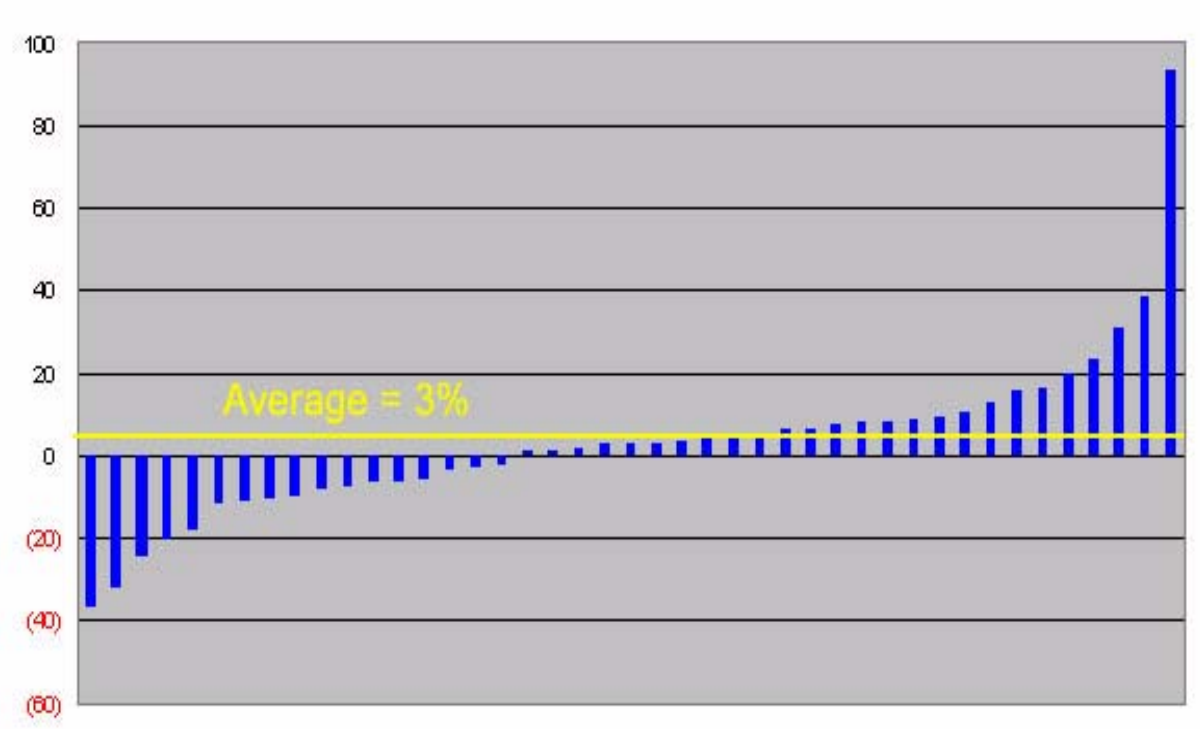

Figure 2: **Spartan-3 Design Performance vs. Cyclone II Performance (ISE 7.1i and Quartus II 4.2_sp1)**

Conclusion

Cyclone II performance as demonstrated by a suite of customer designs using the most cost effective speed grade has degraded almost a full speed grade from Quartus II v4.1 to v4.2, and further degradation is indicated for the new v5.0.

Spartan-3 design performance is now slightly faster than Cyclone II when comparing the most cost effective speed grade in each device.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/24/05	1.0	Initial Xilinx release.