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The Differences Between DataGATE and "Sleep Modes"

By: CPLD Applications

This White Paper discusses the differences between CoolRunner™-II DataGATE™ and various "sleep modes" used by other devices. Both these features are used for low power applications, but, we will show that while DataGATE has many advantages over "sleep modes," the "sleep modes" have no advantages over DataGATE.

CoolRunner-II CPLDs are built on an inherently ultra low power patented technology that reduces standby current to as low as 13 microamps. The technology, known as Fast Zero Power, enables you to build fast, low power handheld consumer devices using programmable logic. DataGATE is an advanced feature of the these devices that enables the design to gate out unwanted signals during actual operation, thus saving addtional power from unwanted toggling of I/Os and downstream logic. You have to ability to select the inputs and outputs for DataGATE, and turn them on and off at will.

Introduction

What is DataGATE?

The patented DataGATE technology was developed to permit a straightforward approach to additional power reduction. Each I/O pin has a series switch that can block the arrival of free running signals that are not of interest. Signals that serve no use may increase power consumption, and can be disabled. Users are free to do their design, then choose sections to participate in the DataGATE function. DataGATE is a logic function that drives an assertion rail threaded through the medium and high-density CoolRunner-II CPLD parts. Designers can select inputs to be blocked under the control of the DataGATE function, effectively blocking controlled switching signals so they do not drive internal chip capacitances. Output signals that do not switch, are held by the bus hold feature. Any set of input pins can be chosen to participate in the DataGATE function. With DataGATE, designers can approach zero power, should they choose to, in their designs.

The main features are:

- Power consumption reduced dramatically, as much as 99% (see **White Paper 227**).
- Pins can be individually selected so that other logic within the device can still be used. Of course, all pins can be selected if nothing is to be used while DataGATE is asserted.
- Logic states are retained.
- DataGATE can be asserted externally, or internally by timer or state machine (see **XAPP395**).
- DataGATE recovery is less than 8.2 ns (see individual **data sheets**).
- DataGATE can also be used as a debugging tool.
- DataGATE requires no external circuitry.

What is Sleep Mode

Sleep Mode and other low power modes are schemes involving powering down the device and turning it back on when needed. It is an on/off switch approach. It differs from DataGATE as shown in Table 1.

Table 1: **DataGATE/Sleep Mode Comparison**

Feature	DataGATE	Sleep Mode
Individual Pin Selection	Yes	No
Device Still Operational	Yes	No
Logic Still Available	Yes	No
On/Off Recovery Time	<8.2 ns	as low as 250 µs
JTAG Programming	Operational	Non-operational
Internal Control	Yes	No
Data/Logic Retention	Yes	Yes on some; no on others
External Components Needed	No	Yes on some; no on others
Quiescent Current	13 µA	40 µA; 110 µA; external clocks must be disabled!

As you can see from the table, sleep modes do not have nearly the advantages of DataGATE, but they do offer similar quiescent current and some vendors have data/logic retention like a CoolRunner-II CPLD. They do not have the same low power as a CoolRunner-II when in actual use, however.

DataGATE Architecture

Figure 1 details the delivery of the DataGATE Assertion Rail throughout the I/O structure of a CoolRunner-II CPLD. This image doesn't convey the generation of the DataGATE activation method, but simply the delivery of the control signal to each input pin, with independent control of whether that pin will participate in the gating action. Specifically, two items should be noted. First, each pin can be programmed to participate in the DataGATE operation or not—the standard default is not to participate. The second aspect is that the individual pass transistors permit signal entry into the CPLD, or blocking of the input pin.

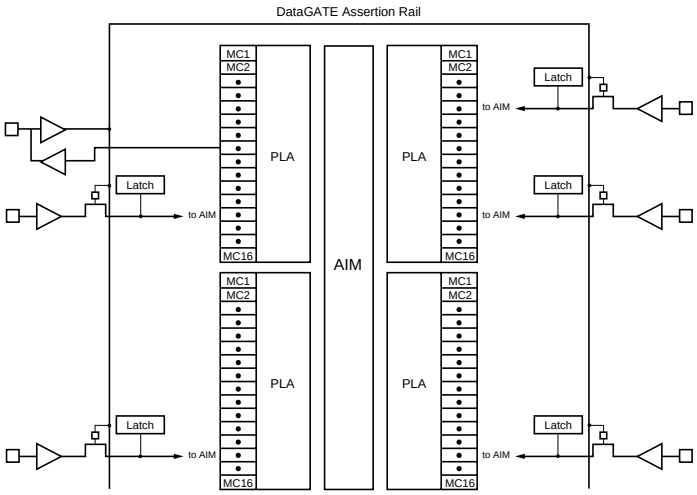

Figure 1: **DataGATE Rail**

Figure 2 expands the detail for a single input pin. If the input pin becomes blocked, the last driven value into the CPLD will automatically be latched and held so a solid binary value is delivered into the CPLD core. It should be noted that the Assertion Rail is driven from a specific macrocell within the CPLD, and that when that macrocell drives high, input data will be blocked at participating pins. If the Assertion Rail is low, data passes freely into the chip. The condition of the DataGATE Assertion Rail is manifested at a specific pin (designated DGE), which will vary from chip to chip within the CoolRunner-II family.

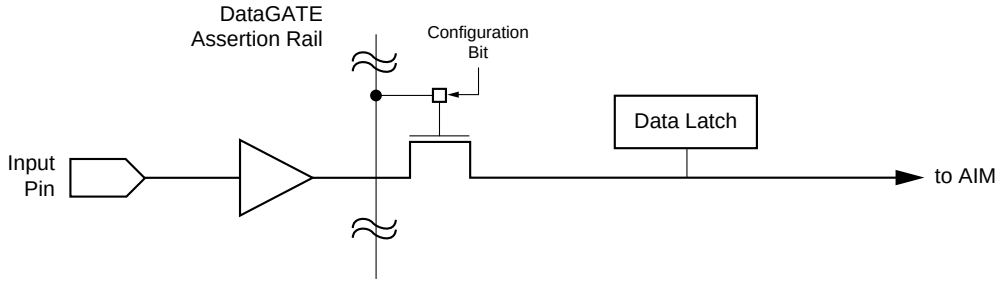

Figure 2: **DataGATE Detail**

Configuring Pins for DataGATE

Applying the DATA_GATE attribute to any I/O pad indicates that the pass-through latch on that device pin is to respond to the DataGATE control line. Any I/O pad (except the DataGATE control I/O pin itself), including clock input pads, can be configured to get latched by applying the DATA_GATE attribute. All other I/O pads that do not have a DATA_GATE attribute remain unlatched at all times. The DataGATE control signal itself can be received from off-chip via the DataGATE/I/O pin, or you can generate it in your design based on inputs that remain unlatched (pads without DATA_GATE attributes).

Any I/O pad (except the DataGATE Enable I/O pin itself), including clock input pads, can be designated to get latched when the DGE pin is asserted. All other I/O pads remain unlatched at all times.

VHDL

To specify DataGATE latching in a VHDL design, instantiate the LDG DataGATE latch from the CoolRunner-II library for each input pad to be latched and pass the input signal through it as follows:

```
component ldg port (d, g: in std_logic; q: out std_logic);
end component;
...
begin ...
u1: ldg port map (d=>my_input, g=>my_enable, q=>my_input_int);
```

Verilog

To specify DataGATE latching in a Verilog design, instantiate the LDG DataGATE latch from the CoolRunner-II library for each input pad to be latched and pass the input signal through it as follows:

```
LDG u1 (.Q (my_input_int), .D (my_input), .G (my_enable);
```

ABEL

To specify DataGATE latching in an ABEL design, assign each input pad to be latched to an internal node using a registered assignment and specifying the enable control using the .LDG dot-extension (in place of a .LE or .LH dot-extension), as follows:

```
my_input_int := my_input;
my_input_int.LDG = my_enable;
```

Schematic

DataGATE can also be applied to a schematic design by placing the **data_gate** attribute on an I/O pad.

Setting the DataGATE Control Pin

When applied to an I/O pad, the BUFG attribute maps the pad to one of the device's global control pins. By setting **BUFG=data_gate**, the I/O pad is set to be the DataGATE control pin.

UCF

In a UCF file, call out the DataGATE control pin as follows:

```
NET signal_name BUFG=data_gate;
```

Schematic

In a schematic design, configure and I/O pin to be a global control pin by placing the following on an I/O pad.

```
BUFG=data_gate
```

ABEL

In ABEL HDL, set the DataGATE control pin as follows:

```
XILINX PROPERTY 'bufg=data_gate signal_name';
```

XST

In the XST synthesis tool, set the DataGATE control pin as follows:

```
attribute BUFG of signal_name : signal is "data_gate";
```

Operating the DataGATE Control Pin

The latch enable (G) input of the LDG latch is active-low. To assert the DataGATE state, drive the LDG latch enable input (the device's DGE/I/O pin) High, which closes the latch and blocks input transitions. To allow data to pass through the latch, drive the LDG latch enable Low.

The D input of each LDG latch must be connected to a device input pad and must have no other fan-outs (must not branch). The CPLD fitter maps the G input to the device's DataGATE Enable control pin (DGE). There must be no more than one DataGATE Enable signal in the design. The DataGATE Enable signal can be received from off-chip via the DGE/I/O pin, or you can generate it in your design based on other inputs that remain unlatched. The DataGATE Enable signal may be reused by other ordinary logic in the design.

Summary

Low power CPLDs are superior to non-volitile FPGAs in meeting power budgets. There are many options available when using low power CPLDs to reduce power consumption. They are designed to be inherently low power devices, but also have additional features within them, including I/O gating, which can dramatically reduce their overall power, when properly applied.

Additional Information

For more information, see:

Xilinx Application Note 436, Managing Power with CoolRunner-II CPLDs

White Paper 227, The Real Value of CoolRunner-II DataGATE

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/31/06	1.0	Initial Xilinx release.