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Forward Error Correction in Digital Television Broadcast Systems

By: Michael Francis and Robert Green

Digital television (DTV) broadcasting is in the process of migrating from analog to digital systems, with regions around the world at different stages of adoption. With some governments looking to auction off the remaining analog spectrum, deadlines have been set for regions to switch off analog TV transmission, resulting in growing demand for flexible technologies to enable a smooth transition in the timescales available. Various delivery systems are available for digital TV, but the main ones are satellite, cable, terrestrial, and mobile. Each has a variety of standards and derivatives that are either mature or emerging. These standards aim to ensure interoperability between different vendor's equipment, including the set-top boxes, cell phones, and other means for DTV reception.

Each region has their own requirements for a DTV delivery system, dependent on many factors, such as bandwidth available in the digital spectrum, the

terrain—whether it is flat, mountainous, or a dense city center—or to add interactivity, perhaps for education or medical services in a developing country. All of these mean that one size does not necessarily fit all when it comes to the delivery mechanism. However, there remain similarities in the methods used to prepare video, audio, and data for wired or wireless communication, with all of these systems relying on Forward Error Correction (FEC) techniques to ensure that any data lost during transmission can be reconstructed at the receiver.

This white paper gives an overall view of the various mainstream digital television standards and outlines related Forward Error Correction solutions available from Xilinx for cable, satellite, terrestrial, and mobile systems.

Introduction

The major worldwide standards for DTV broadcasting are:

- Digital Video Broadcasting (DVB)
- Advanced Television Systems Committee (ATSC)
- Integrated Services Digital Broadcasting (ISDB)
- Data Over Cable Service Interface Specification (DOCSIS) J.83 A/B/C
- Digital Multimedia Broadcasting (DMB)

Even though these standards all have differing modulation schemes and data rates, they all share a requirement for error correction. Forward Error Correction (FEC) is widely used in digital television systems for the reliable transmission of audio, video, and data. FEC has a number of objectives:

- To enable a receiver to detect and correct errors automatically without requesting retransmission
- To add redundant parity information to the data at the transmitter
- To manipulate data to reduce susceptibility to different noise types
- To optimize the use of available bandwidth

Standards Overview

Digital Video Broadcasting (DVB)

The DVB Project is an alliance of around 260 worldwide companies comprising of broadcasters, manufacturers, network operators, and regulatory bodies. Their objective is to agree to flexible and interoperable specifications for digital broadcasting systems. The main baseline DVB standards are listed below.

Table 1: **Main Baseline DVB Standards**

Standard	Description	Number
DVB-S	Satellite	EN 300 421
DVB-S2	Satellite	EN 302 307
DVB-C	Cable	EN 300 429
DVB-T	Terrestrial	EN 300 744
DVB-H	Handheld Terrestrial	EN 300 304

There are over 100 standards and recommended practices related to DVB, available from ETSI, with new standards constantly being released for new and improved delivery methods (for instance, the latest to be ratified is the DVB-SH standard for satellite distribution to handhelds, based on a turbo code FEC and working with terrestrial repeaters for indoor coverage). This paper concentrates on the mainstream broadcast methods to outline the variety of forward error correction techniques used, the commonality between many which often allows fundamental FEC elements to be modified through parameterization, and the use of FPGAs to support the evolving needs of these systems.

DVB-T (Terrestrial) System

The DVB-T system [Ref 1] is the terrestrial transmission system of the DVB standards. The block diagram for a DVB-T transmitter is shown in Figure 1. Source data, consisting of video, audio, and data, is multiplexed into MPEG transport stream (TS) packets. Each packet is 188 bytes long with 184 bytes for data and 4 bytes for header information, such as synch and packet ID bytes.
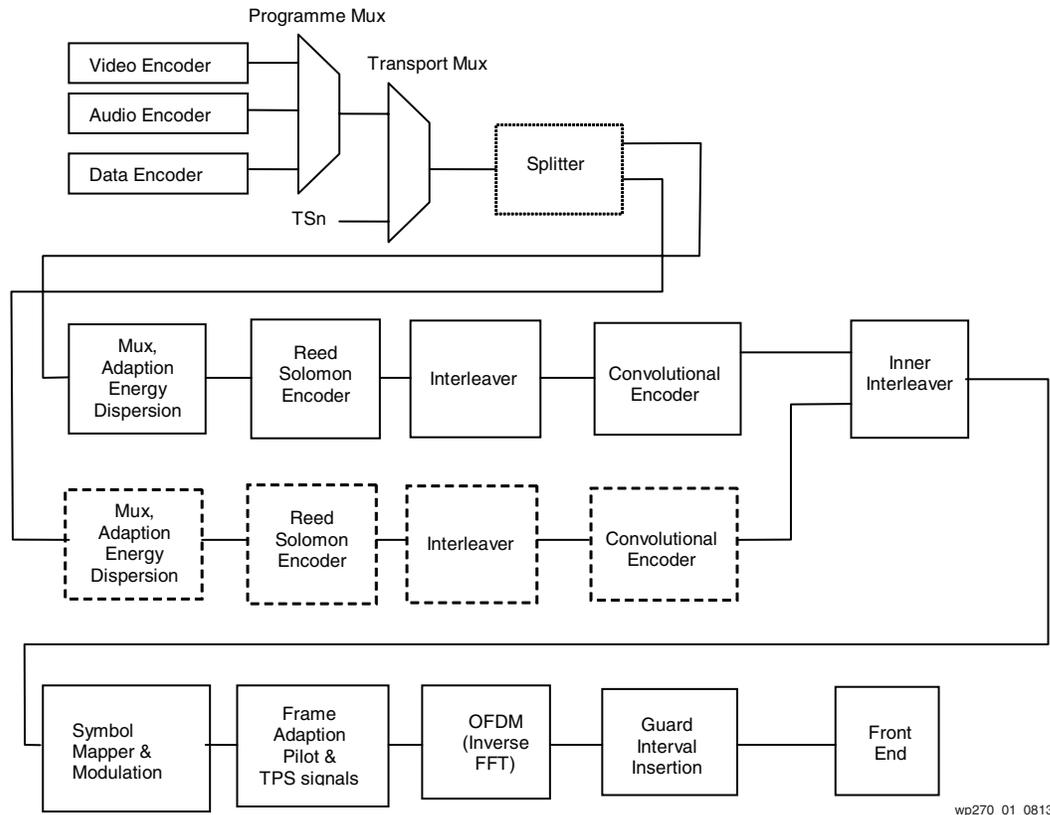
Figure 1: ***DVB-T Transmitter***

The packets go through an energy dispersal process. The transport stream packets are combined with the data stream from a pseudorandom noise generator as shown in Figure 2. This is basically a feedback shift register. There are two main reasons for the scrambling of the input packets. First, it helps with the timing recovery circuit of the receiver, removing long sequences consisting of '0' or '1' only; and, second, it stops the concentration of too much power in a narrow frequency band. The concentration of power in a narrow band can interfere with adjacent channels due to cross modulation and intermodulation. The synchronization byte of the packet is not changed.
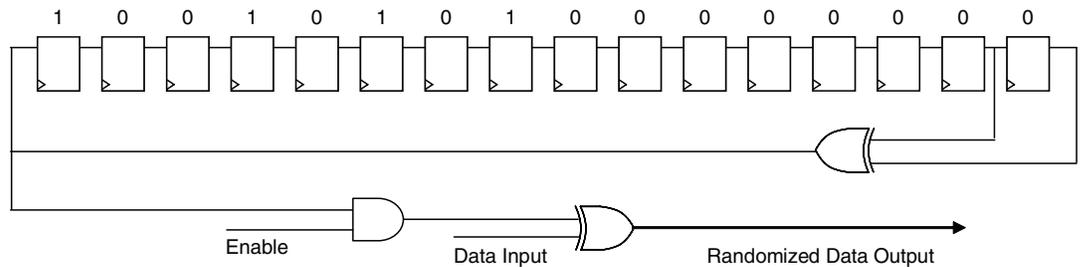
Figure 2: ***DVB PRBS Scrambler***

For error protection, a concatenated forward error correction (FEC) scheme is used. The randomized TS packets are encoded by the Reed-Solomon (R-S) Encoder using a (n, k) code; where n is the block size and k is the number of information symbols. In this case, n is 255 symbols and k is 239 symbols, and a symbol represents 8 bits. This means that 16 check symbols are appended to the information bytes. This code allows up to 8 symbols of data to be corrupted and still be corrected, that is a total of 64 bits. As the transport stream packets are only 188 bytes long, the first 51 bytes are set to

zero, but are not transmitted. Therefore, it is actually a shortened (204,188) code. The Reed Solomon scheme corrects random errors where only a few bytes of data are lost during transmission.

The data is then applied to an outer interleaver. The purpose of the interleaver is to spread long burst errors across several data packets and improve the BER performance by making it easier for the R-S decoder to correct errors. The interleaver uses a convolutional approach known as the Forney algorithm. The interleaver has 12 branches of shift registers to perform the interleaving, and a delay of 17 as shown in Figure 3.
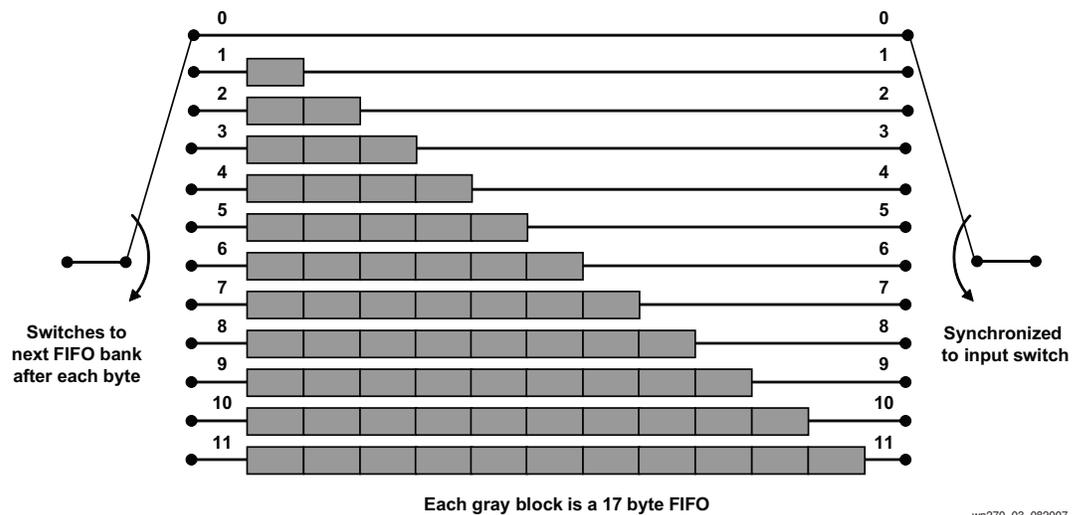

Switches to next FIFO bank after each byte

Synchronized to input switch

Each gray block is a 17 byte FIFO

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Figure 3: **Interleaver**

Inner error protection is provided by convolutional encoding. A convolutional encoder with code rate 1/2 is used. This means for every input bit, two output bits are generated. The implementation consists of XOR gates and shift registers and is simple logic. To reduce the number of bits transmitted, various puncturing schemes are used which discard selected bits from the encoder output. Typical puncture rates are 2/3, 3/4, 5/6, and 7/8. For instance, a 3/4 puncture rate means that for every 3 input bits, 4 output bits are transmitted from the encoder output rather than the 6 bits that are actually generated. Puncturing can be implemented using external logic to the convolutional encoder. This allows the freedom to change between the various puncture rates.

The next section is the inner interleaver. It consists of a bit and symbol interleaver. The purpose is to change the sequence of the symbols to distribute any errors that might get introduced in the transmission channel, which is achieved by another pseudorandom generator.

The mapping/modulation process is next, and a choice can be made between Quadrature Phase Shift Key (QPSK), Quadrature Amplitude Modulation (QAM)16-QAM and 64-QAM allowing tradeoff between transmission data rates and signal robustness. QAM conveys data by changing, dependent on the input data to be transmitted, the amplitude of two carrier signals which are 90 degrees out-of-phase with each other. Phase-shift keying is similar to QAM, but the amplitude of the modulating signal is constant, only the phase varies dependent on input data.

To help in the reception of the signal being transmitted on the terrestrial radio channel, additional signals, known as Pilot and Transmission Parameters Signaling (TPS) are inserted in each block. Pilot signals are used during the synchronization and

equalization phase, while TPS signals are used to send the parameters of the transmitted signal and to identify the transmission cell. It should be noted that the receiver must be able to synchronize, equalize, and decode the signal to gain access to the information held by the TPS pilots. Thus, the receiver must know this information beforehand, and the TPS data is only used in special cases, such as changes in the parameters, resynchronizations, etc.

The transmission of the information bits is performed by Coded Orthogonal Frequency Modulation (COFDM). The symbols are created by an Inverse Fast Fourier Transform (IFFT). Two options are available in DVB-T systems for the number of carriers: 2k or 8k. This defines the number of points for the IFFT and the choice of carrier number depends on the tradeoff made between robustness of signal and the extra signal strength required. The 8k mode was introduced, as it is more suitable for single frequency networks where clusters of transmitters cover the same region. The COFDM symbol is preceded by a guard interval so as to deal with multi-path effects.

The final stage in the transmission is the RF modulation where the digital signal is transformed into an analog signal, using a digital-to-analog converter (DAC), and then modulated to radio frequency by the RF front-end. The occupied bandwidth is designed to accommodate each single DVB-T signal into 6, 7, or 8 MHz wide channels.

The DVB-T standard also allows the use of hierarchical modulation. Two independent data streams can be transmitted using different paths through the early part of the concatenated FEC (as shown by the dotted blocks in Figure 1) and different modulation schemes. An example is QPSK for high priority and 16-QAM for low priority. The high priority stream, with the lower data rate can be received in an environment of low carrier-to-noise ratio. The low priority stream, with the higher data rate, would be used in environments with a higher carrier-to-noise ratio. In fact, one of the original intentions of the hierarchical mode was to transmit high definition (HD) channels with lower priority alongside standard definition (SD) channels with the higher priority, allowing receivers to fall back to an SD transmission should the HD signal be lost. Adoption of this scheme seems to be very limited currently, but may well be taken advantage of in the future.

The DVB-T receiver is shown in Figure 4. After the conversion from RF to digital domain, the guard interval is removed. The Orthogonal Frequency Division Multiplex (OFDM) demodulator is performed by a forward Fast Fourier Transform (FFT), and the Transmission Parameters Signal (TPS) is removed. After de-mapping, the information data is decoded by the inner decoder.

The inner decoding function is performed by a Viterbi decoder. The Viterbi decoder has a constraint length of 7 and uses polynomials 171 (octal) and 133 (octal). To handle the puncture rates, as specified by the standard, puncturing is performed external to the Viterbi decoder, and in place of the missing symbols, null symbols can be inserted along with an erase input to indicate the position of the null symbols.

The format of the input data to the Viterbi decoder can either be hard or soft coding. The soft coding format tends to give a better bit error rate (BER) performance, because it gives a confidence value for each bit ranging from a maximum confidence zero to a maximum confidence one. The computation of the soft data is done using the Log Likelihood Ratio (LLR). The I and Q data from the demodulator are used to create the confidence value. The calculation is done by calculating the minimum distance from the received symbol to all the possible transmitted symbols and then calculating the probability that a particular bit is either a zero or a one.

The data from the Viterbi decoder is de-interleaved before the block data is sent to the R-S decoder.

The R-S decoder has the same (204,188) code as the transmitter and can give indications of the number of errors and how many bits have changed from ones to zeroes and vice versa. The transport packets are then recovered.
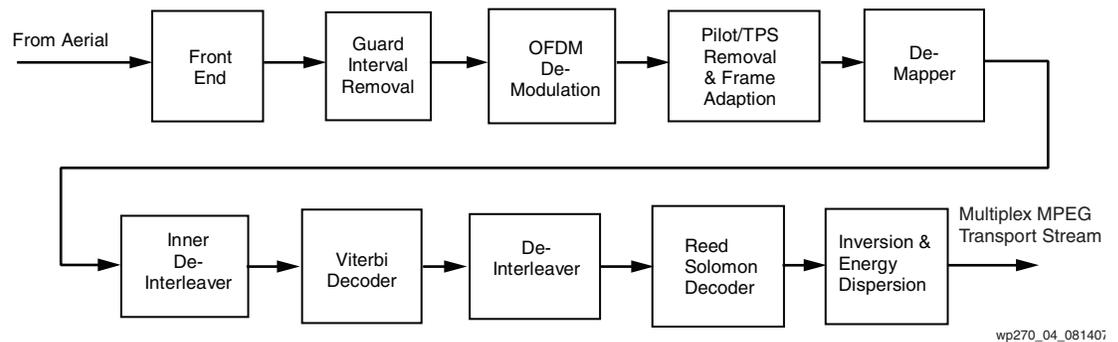

Figure 4: **DVB-T Receiver**

DVB-S (Satellite) System

The DVB-S system [Ref 2]uses similar FEC components as DVB-T error protection. It has less overall complexity as it does not require the use of OFDM to overcome reflections and interference due to terrain. The transmitter is shown in Figure 5.
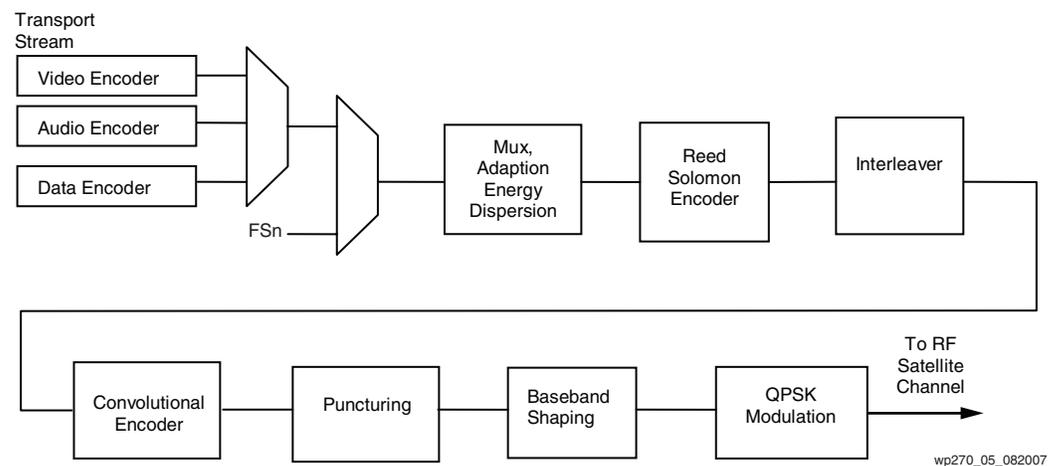
Figure 5: **DVB-S Transmitter**

As per the DVB-T system, the video, audio, and data input streams are multiplexed into an MPEG-2 Transport Stream. The outer code is a shortened R-S (204,188) code, allowing the correction of up to a maximum of 8 erroneous bytes for each 188-byte packet. The interleaver rearranges the transmitted data sequence in such a way that it becomes more rugged to long sequences of errors. Inner error protection is provided by convolutional encoding as before. The DVB-S system has a number of puncture schemes based on ½ code rate and these are 2/3, 3/4, 5/6, and 7/8. The mapping is done into QPSK, which is then processed through baseband shaping with a Finite Impulse Response (FIR) based raised-cosine shaped filter to remove inter-signal interference (ISI) at the receive side. ISI is typically the result of reflections on the signal which cause either constructive or destructive interference between the currently received signal and a previously transmitted one, depending on phase. The I and Q values of the QPSK signal are finally modulated to radio frequency by theRF front-end for a 36-MHz satellite transponder to give approximately 45 Mbps data rate.

Figure 6 shows the satellite receiver. The QPSK demodulator performs the down conversion function to produce the real and imaginary data. The matched filter uses

FIR filters to perform the receive pulse shaping. I and Q data are converted to soft decisions for the Viterbi decoder, also known as the *inner* decoder. Even though the Viterbi decoder can do *hard* decision coding, a better BER performance is achieved with soft decisions. De-interleaving is followed by the R-S decoder, or *outer* decoder which is the second layer of protection. The data is recovered from the random pattern introduced in the transmitter to create the original video/data packets.
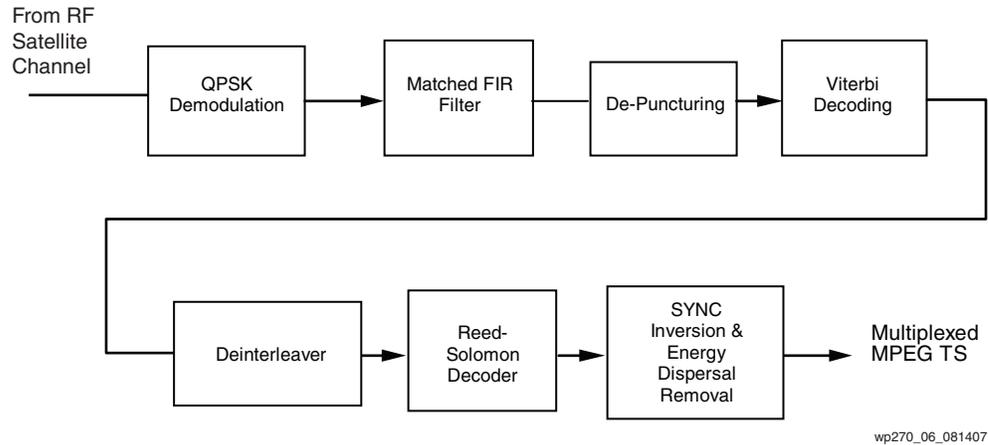

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Figure 6: **DVB-S Receiver**

DVB-S2 (Satellite) System

DVB-S2 [Ref 3] is the second generation scheme for satellite communications which has a number of improvements and yet is still backward compatible with DVB-S. The improvements are increased system capacity, up by 40 percent, enhanced error protection, and the ability to support multiple input formats and transport streams. The error correction is improved so much that DVB claims the signal-to-noise ratio (SNR) approaches the Shannon limit—a theoretical limit which states the maximum possible data capacity for a transmission channel. Figure 7 shows the second generation satellite transmitter.

The multiple input streams go through mode and stream adaptation to create baseband frames (BBFRAME) before being scrambled. FEC encoding is a concatenation of the Bose-Chaudhuri-Hochquenghem code (BCH), Low Density Parity Check (LDPC), and a bit interleaver. The FEC block length is either 64 800 bits, or 16 200 bits. The reason for the BCH code is to avoid error floors at low bit error rates. The use of this particular concatenation FEC scheme is what ensures error protection close to the Shannon limit.
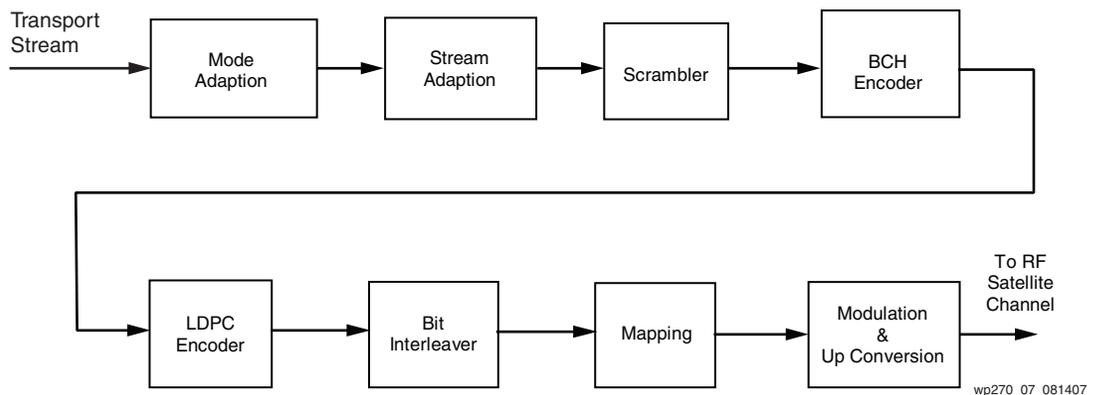

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Figure 7: **DVB-S2 Transmitter**

The mapping formats supported are QPSK, 8PSK (Phase Shift Key), 16 APSK (Amplitude Phase Shift Keying) and 32 APSK. Code rates of 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, and 9/10 are used. The signal goes through up conversion and modulation to the RF satellite channel.

The receiver is shown in Figure 8. The RF signals are demodulated and down converted to produce real (I) and imaginary (Q) data, and the remainder of the process to obtain the MPEG TS is basically the inverse of the transmission side.
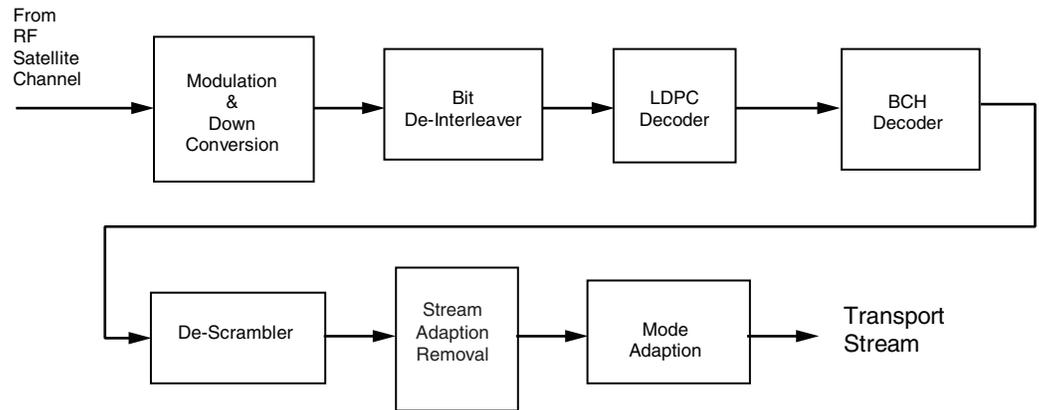

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Figure 8: **DVB-S2 Receiver**

DVB-C (Cable) System

The DVB-C [Ref 4] transmitter is exactly the same as the DVB-S system up to the interleaver output and is shown in Figure 9. For Byte/m-tuple conversion, the data bytes are encoded into bit m-tuples where m is 4, 5, 6, 7, or 8. The differential coding block takes the two most significant bytes in each m-tuple and encodes in order to give some ruggedness to the signal. Then the mapping is done into either 16-QAM, 32-QAM, 64-QAM, 128-QAM, or 256-QAM. The QAM (Quadrature Amplitude Modulation) signal is filtered with a raised-cosine shaped filter to remove ISI. The I and Q values are finally modulated to radio frequency by the RF front-end for an 8 MHz cable channel to gives approximately 38-40 Mbps data rate.
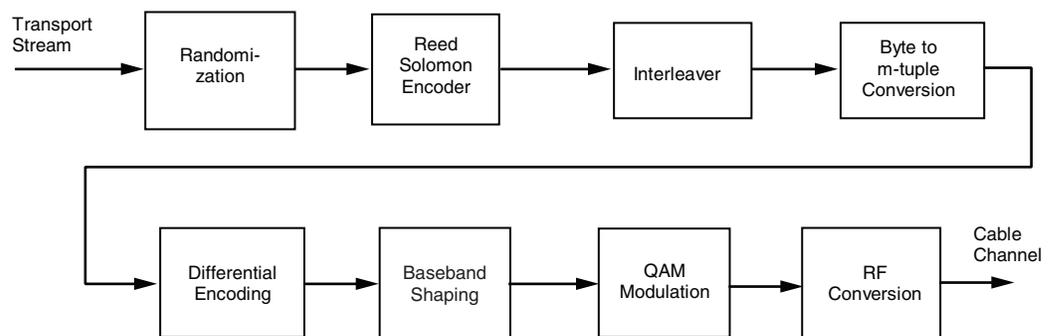
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Figure 9: **DVB-C Transmitter System**

The receiver is shown in Figure 10. After demodulation, the I and Q signals go through a matched filter and through to the FEC coding sections consisting of the de-interleaver and the R-S decoder.
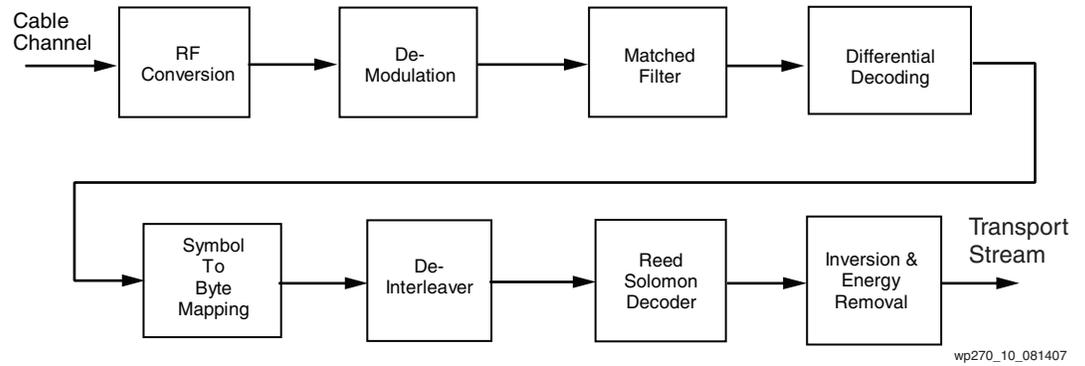
Figure 10: **DVB-C Receiver System**

DVB-H (Handheld) System

DVB-H [Ref 5] is a technical specification for bringing broadcast services to handheld receivers. The standard is based on the DVB-T terrestrial specification and uses the OFDM transmission system. The additional features are:

- Multi-Protocol-Encapsulation (MPE). The input data for DVB-H is Internet Protocol (IP) packets, and these are encapsulated into the TS streams for DVB-T transmission.

- Time-slicing. Since handheld receivers have a limited battery life, time slicing is used to reduce power consumption.

- An extra 4k network mode, providing a 4k carrier option for OFDM

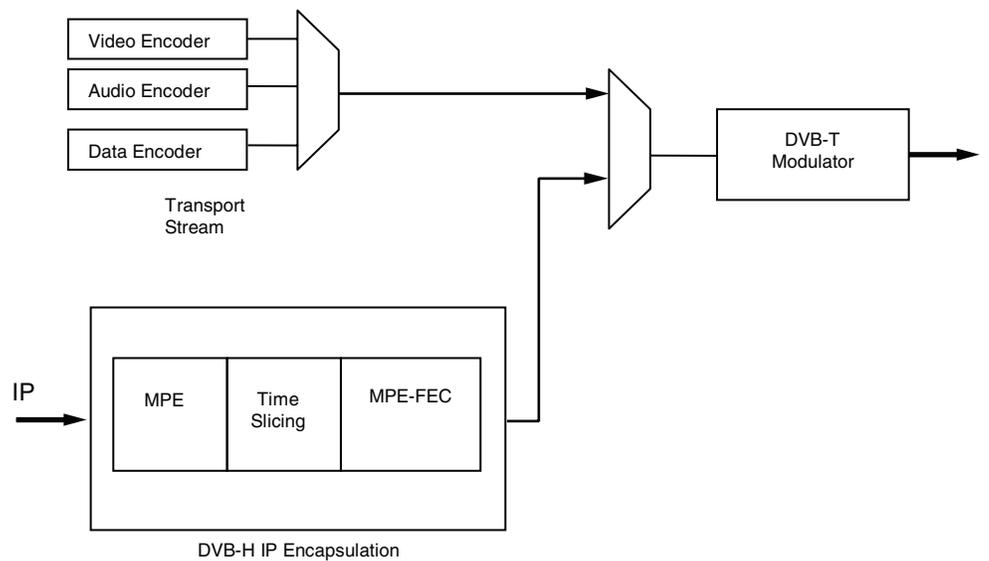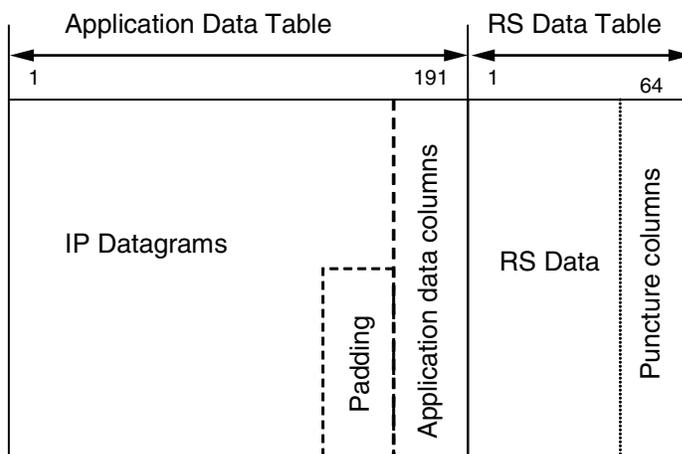- MPE-FEC. Protection using multi-protocol encapsulated FEC (MPE-FEC)

See Figure 11.

Figure 11: **DVB-H System**

MPE-FEC uses an FEC frame which is made up of 255 columns and up to a maximum of 1024 rows, as shown in Figure 12. The frame is split into two sections: an *application table*, using 191 columns; and an *RS data table* using the other 64 columns for parity data.

*Figure 12:* **DVB-H FEC Frame**

The application table is where the IP data is stored and any unused positions are padded with zeros. The IP data is written to the application table column-by-column. However, the R-S code (255,191) is applied on a row-by-row basis.

There is also the provision within the specification to only transmit some of the parity data to allow puncturing. At first glance, the R-S code (255,191) allows the correction of up to 32 symbols. However, the FEC frame utilizes CRC-32 checking, so when the data is received in the receiver the data is marked as *reliable* or *unreliable*. Thus, the positions of the erroneous data are known. This information can be sent to the R-S decoder, via the erasures input to indicate to the R-S decoder where the errors are, and up to 64 symbols can be corrected.

Advanced Television Systems Committee (ATSC)

Established in 1982, the Advanced Television Systems Committee is the group that developed the ATSC digital television standard [Ref 6] for the United States, also adopted by Canada, Mexico, and South Korea.

An ATSC transmitter is shown in Figure 13. The transmitter receives 188 bytes of packetized data/sync (i.e., video/data/audio) and randomizes the data to achieve a flat noise-like spectrum. This random data allows the clock recovery loops in the receiver to retrieve the clock signal.
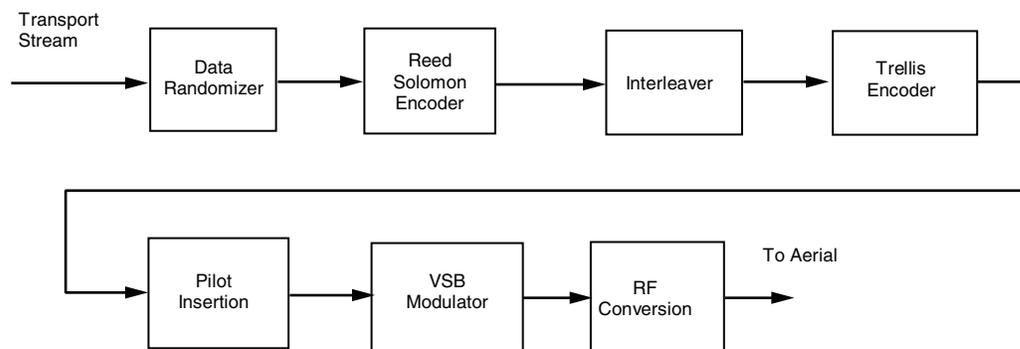
Figure 13: **ATSC Transmitter System**

The R-S encoder provides burst noise protection by appending 20 bytes at the end of the 187 data packets for the (207,187) code. The data is interleaved before being

applied to a trellis encoder. For trellis coding, each incoming byte is split up into a stream of four, 2-bit words. For every 2-bit word entering the encoder, 3-bits are output based on the past history of previous incoming 2-bit words. In other words, it is a 2/3 rate coder. These 3-bit output codes represent the eight level symbols of 8-VSB (Vestigial Sideband) modulation.

Following pilot insertion, the signal is input to an 8-VSB or 16-VSB modulator. For 16-VSB, intended for cable systems, the trellis encoder is not used. In fact for cable systems, QAM has become a widely used replacement for the 16-VSB scheme. 8-VSB provides trellis coded 19.39 Mbps for terrestrial transmission over a 6 MHz. 16-VSB is capable of 38.78 Mbps over a 6 MHz cable channel. The modulator output is fed into a root-raised cosine filter before being applied to the RF front end.

Just for reference, Figure 14 shows the difference between an 8-VSB and 64-QAM constellation. The QAM scheme shows 64 different points of phase and amplitude dependent on the input data stream and sampling needs to be done on real (I) and imaginary (Q) symbols. The 8-VSB scheme shows the 8 levels of the sidebands on the I axis, with sampling on the Q symbols unnecessary as they don't convey data. The aim is to make reception and sampling somewhat less complex.
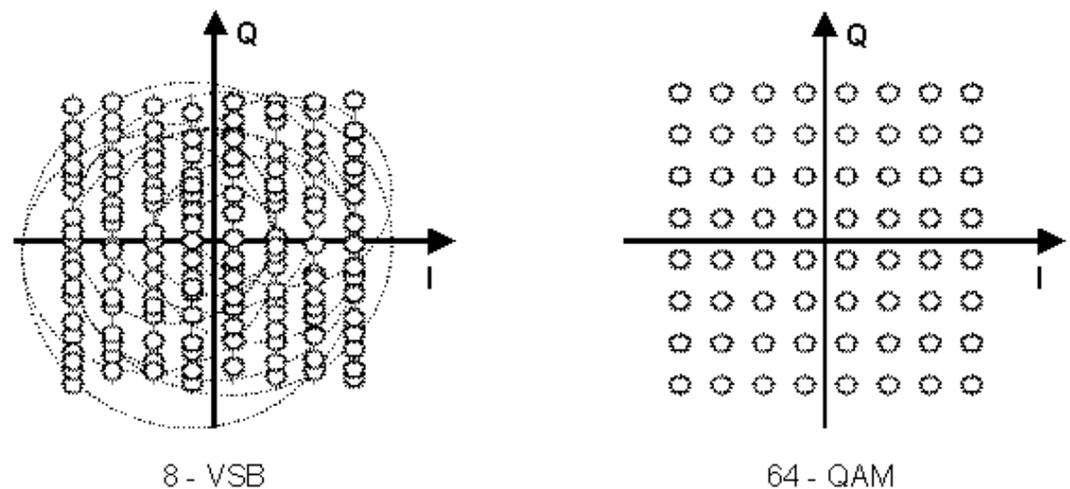

Figure 14: **8-VSB vs. 64-QAM [Ref 7]**

The receiver is shown in Figure 15 and is basically the reverse of the transmitter scheme. The receiver uses clock recovery to extract a reference clock and an equalizer to deal with any distortion due to multipath effects. The subsequent sections are the concatenated FEC consisting first of trellis decoding. The trellis decoder uses the received 3-bit codes used in 8-VSB to reconstruct the changing data stream from one 2-bit word to the next, discarding potential errors based on the signal's past and future behavior. The remaining blocks are the de-interleaver and R-S decoder, which work in similar ways to previous systems mentioned and with codes that match the transmitter.
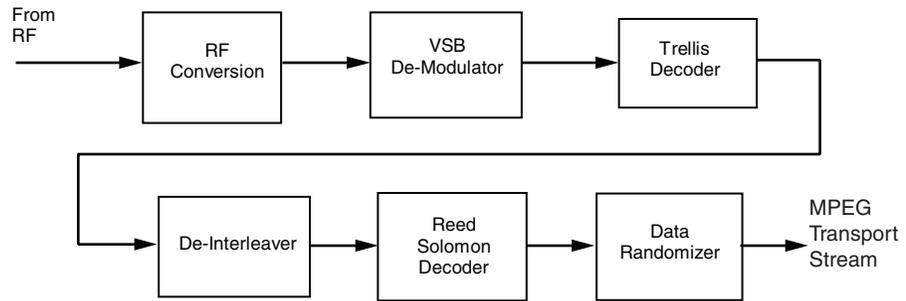
Figure 15: **ATSC Receiver System**

Integrated Services Digital Broadcasting (ISDB)

ISDB is the set of Japanese standards that covers terrestrial (ISDB-T [Ref 8]), satellite (ISDB-S [Ref 9]) and cable (ISDB-C) communication. Multiple transport streams are re-multiplexed into a single transport stream. The TS is first processed through an R-S encoder with (204, 188) code. A key feature of ISDB is hierarchical transmission. The TS packets are divided into sets of packets according to program information, into a maximum of three parallel processing sections, known as hierarchical separation (A, B, C). Each section performs energy dispersal, byte interleaving and convolutional encoding. The convolutional encoder could have different coding rates, and different modulation scheme (D, E, F). The transmission system is shown in Figure 16.
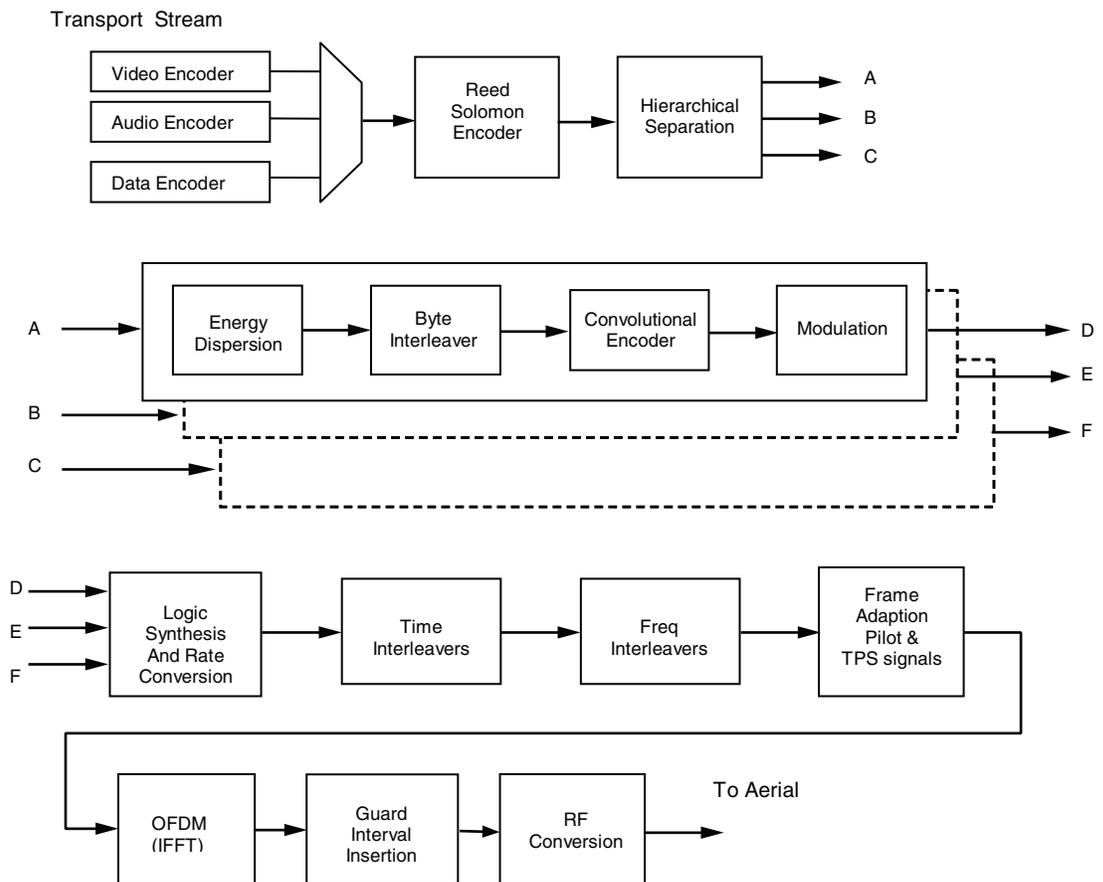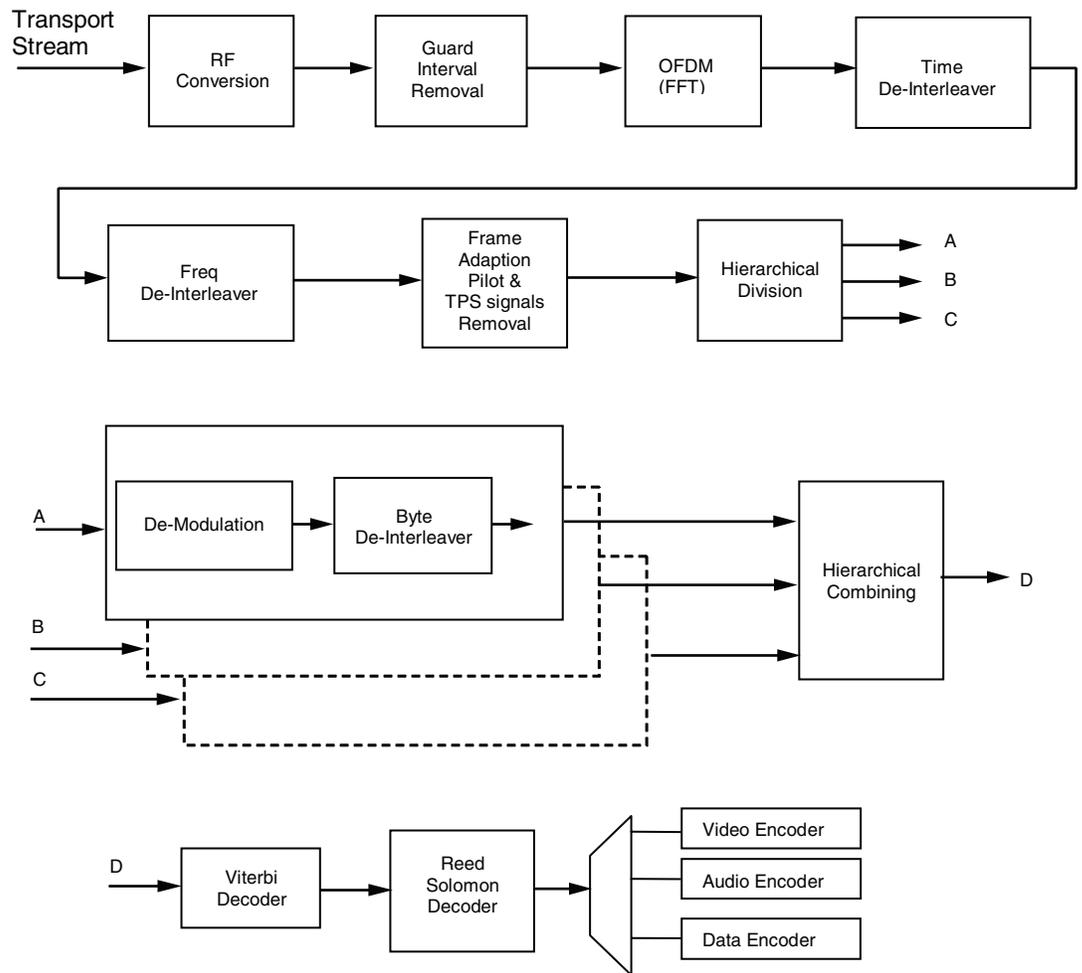

Figure 16: **ISDB Transmission System**

The modulation scheme used is Band-Segmented Transmission OFDM (BST-OFDM). The transmission band consists of OFDM segments each with a bandwidth of approximately 430 kHz. There is a maximum of 13 segments to give a total bandwidth of 5.6 MHz. Similar to DVB systems, the ISDB specification allows for three modes of transmission: 2k, 4k, and 8k. ISDB-S also defines the 204 byte code length used in R-S encoding and is combined with BPSK, QPSK, and Trellis-coded 8PSK (TC8PSK). ISDB-T uses QPSK, Differential QPSK, 16-QAM, and 64-QAM, whereas ISDB-C uses 64-QAM only.

Reception is basically the reverse process and uses similar concatenated FEC blocks as other schemes, such as DVB, but with hierarchical modes needing to be determined and the correct FEC parameters used appropriately. The receiver block diagram is shown in Figure 17.

Figure 17: **ISDB Reception System**

Data Over Cable Service Interface Specification (DOCSIS)

The DOCSIS suite of specifications [Ref 10] was developed at Cable Television Laboratories (Cable Labs) in Louisville, KY, USA and has been adopted by both the ANSI-accredited standards body the Society of Cable Telecommunications Engineers (SCTE), and the International Telecommunication Union (ITU).

J.83 Annex A/C

The main cable digital standards are J.83 A/C mainly for Europe, and J.83 B for US. The system diagram for annex A/C is shown in Figure 18.
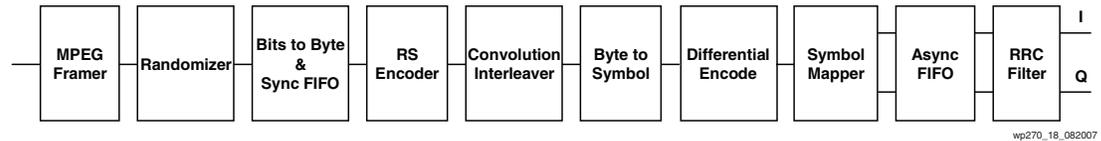

Figure 18: **J.83 A/C Transmission System**

Following the energy dispersal randomization process, systematic shortened R-S encoding is applied to each randomized MPEG-2 transport packet. A (259, 239) encoder is used, with extra bytes discarded after coding to result in a shortened code word (204, 188). The R-S coding is capable of correcting up to 8 erroneous bytes per transport packet. Convolutional Interleaving based upon the Forney approach, with depth I = 12, is applied to the error-protected packets, leaving the periodicity of the sync bytes in an interleaved frame (of 204 bytes) unchanged. These bytes are further converted into QAM symbols.

J.83 Annex A allows for 16-, 32-, and 64-QAM constellations and permits extensions to higher constellations, such as 128- and 256-QAM as per the DVB-C specification. J.83 Annex C allows for a 64-QAM constellation only.

J.83 Annex B

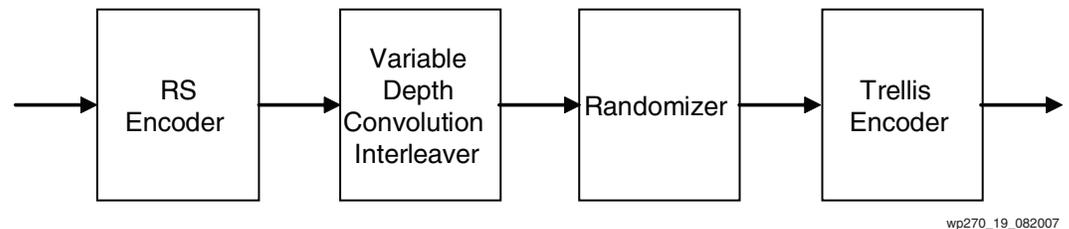The FEC layer uses a concatenated coding technique with four processing layers as shown in Figure 19.

Figure 19: **J.83 B Transmission System**

The Reed-Solomon encoder uses (128,122) code and is capable of correcting up to three symbol errors per R-S block, with a symbol being 7 bits. The same R-S code is used for 64 and 256 QAM. A standard R-S (127,122) code is used with an additional extended parity symbol (the 128th symbol) based on all 127 symbols. The R-S encoder is followed by a variable depth convolutional interleaver to provide error protection against burst noise induced errors. The interleaver operates in two separate modes: Level 1 and Level 2. When operating in Level 1, a single interleaving depth (I=128, J=1) is supported. Level 2 allows variable interleaving depth for 64 and 256 QAM. The interleaver is followed by a randomizer which provides even distribution of the symbols in the constellation. Randomization is not carried out on a FEC frame trailer. An FEC frame comprises 60 R-S frames followed by a 42-bit sync trailer for 64 QAM and 88 R-S frames followed by a 40-bit sync trailer for 256 QAM. The inner code used in this FEC encoder is a Trellis Coded Modulator (TCM). For 64 QAM, TCM generates five QAM symbols for every 28 bit sequence it receives. This set of 28 bits forms a trellis group which is divided into two subgroups, A and B. TCM employs Differential Precoding followed by 4/5 punctured binary convolution code on the LSBs of the A and B subgroups. The overall code rate is 28/30 for 64 QAM. Similarly, for 256 QAM,

TCM generates five QAM symbols for every 38-bit sequence it receives. The overall code rate is 38/40 for 256 QAM.

Digital Multimedia Broadcasting (DMB)

T-DMB

T-DMB [Ref 11] [Ref 12]was derived from the European DAB digital radio standard and has been modified for multimedia reception on portable or mobile device.
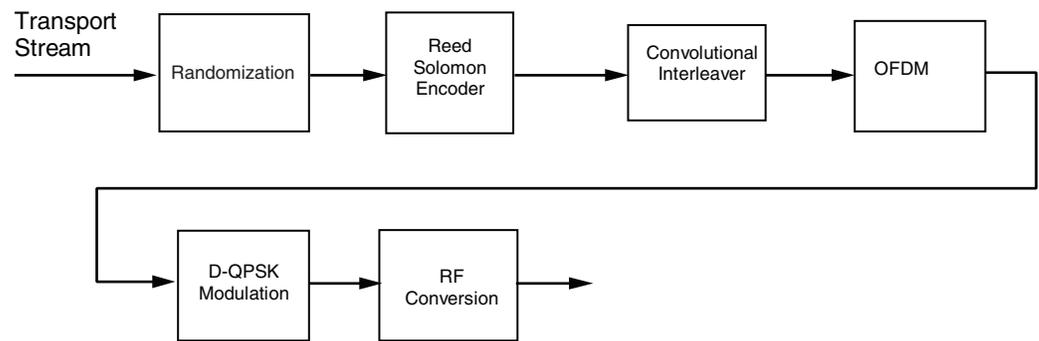

Figure 20: **T-DMB Transmission System**

The error protection in T-DMB consists of two layers; R-S encoding/decoding and convolutional interleaving. As in DVB systems, the R-S code is (204,188) and the interleaver uses a Forney algorithm with the same interleaving depth (I=12). DMB supports OFDM transmission of 2k, 1k, 512, and 256 modes and modulation is implemented with differential QPSK.

Three T-DMB frequency blocks have been assigned to each of the 6 MHz TV channels. Each of the T-DMB blocks can have a multiplexed ensemble with a number of video and audio channels.

T-DMB has been adopted by its home nation South Korea, but is undergoing trials throughout the world.

DMB-T/H

DMB-T/H [Ref 13] is one of the latest DTV standards, developed for the People's Republic of China (PRC) and based on work at Tsinghua University in Beijing and Jiaotong University in Shanghai. Due to its emerging status, it is also known by other names: CDMB-T and DTMB.

One key difference between Korea's T-DMB and China's DMB-T/H is that T-DMB uses multiple, smaller channels at lower bandwidth and must use spectrum for channel separation; DMB-T/H uses wider channels at higher bandwidth for better spectrum efficiency, but at a potentially higher receiver cost. A difference to other DTV transmission standards is the support of two different modulation schemes: time-domain synchronous OFDM (TDS-OFDM), which is a variant of the OFDM scheme used in DVB-T, and ADTB-T which uses 8-VSB like the ATSC system. While maintaining data rates as high as 32 Mbps to cater to multimedia services, TDS-OFDM is designed for better synchronization of mobile and burst data broadcasting and allows an 8-MHz DTV channel to be reused for cellular network applications.

Using TDS-OFDM, transmission signals are separated into two parts: synchronization signals, used primarily for channel selection, and signals that carry actual programs. QPSK, 16-QAM, and 64-QAM modulation are used.

Forward Error Correction Solutions from Xilinx

Despite the number of standards that exist for digital TV broadcast systems, there is a high degree of commonality between them in the variety of FEC sub-blocks used. Many blocks, such as Reed-Solomon and convolutional coding are used in all systems, even in proprietary modulation schemes such as MediaFLO [Ref 14], but use differing codes and other parameters as part of the standardization of the error correction scheme.

Xilinx is able to offer these various FEC sub-blocks as parameterizable IP cores which can be implemented in both Virtex™ and Spartan™ FPGA families. This approach provides a number of benefits:

- Ability to tailor a forward error correction scheme to your exact requirements
- Allow the user to change the parameters of the cores to suit regional variations or adapt to geographical limitations
- Enable the user to reprogram devices after deployment during the evolution of new DTV standards
- Offer high DSP performance and I/O bandwidth to enable optimum throughput of data despite the overhead added by FEC schemes
- Enable system-on-chip integration of multiple channels, saving overall cost (in terms of materials, PCB area and power management, etc.) and offering lowest cost-per-channel versus competing solutions
- Enable integration of other system requirements, such as data and traffic management, operating systems, remote monitoring and self-test, and even codecs, to name a few examples.

To support the FEC requirements as outlined in this paper, there are a number of sources for the IP cores Xilinx can offer. The primary source is the Xilinx LogiCORE™ IP library which contains the following FEC cores:

- Reed-Solomon Encoder
- Reed-Solomon Decoder
- Convolutional Encoder
- Interleaver/De-interleaver
- Viterbi Decoder
- DVB-S2 FEC Encoder

The LogiCORE IP library allows easy configuration of the IP to meet the specifications and they have been developed and designed to work in both our traditional FPGA development systems and also the latest MATLAB® DSP environments.

Xilinx also has many third party partners who offer FEC and complete modulation solutions targeted to Xilinx FPGAs and for use specifically in digital TV broadcast systems. Details of these are available in documentation from our IP Center at www.xilinx.com/ipcenter, or alternatively at the broadcast section of the Xilinx website at www.xilinx.com/broadcast. Many of the cores are available for use in the Xilinx ISE™ development software, and by the use of evaluation licenses have the ability to be run on hardware platforms.

The following section focuses on the technical specifications of Xilinx FEC cores that can be used in digital TV systems.

Xilinx FEC Solutions

Reed-Solomon Encoder and Decoder

Reed-Solomon encoders and decoders are licensed cores that are available via the LogiCORE IP library. The full feature list is:

- Supports all known Reed-Solomon coding standards
- Fully synchronous design using a single clock
- Supports continuous input data with no gap between code blocks
- Symbol size from 3 to 12 bits
- Code block length variable up to 4095 symbols
- Code block length can be dynamically varied on a block-by-block basis
- Supports shortened codes
- Supports error and erasure decoding
- Supports puncturing (as in IEEE 802.16d)
- Supports multiple channels
- Parameterizable number of errors corrected
- Supports any primitive field polynomial for a given symbol size
- Counts number of errors corrected and flags failures
- User-selectable control signal behavior

For implementation of R-S encoders and decoders for the various standards outlined in this paper, the LogiCORE IP library allows the easy configuration for the core via a GUI. Standards like DVB and ATSC can be selected via a drop down menu, so that all the default code and generator polynomials are selected automatically. Other standards can be supported through manual manipulation of the many parameters available for modification. With the high performance and multi-channel capability of the R-S encoders/decoders, very efficient implementations can be achieved.

Further details on the architecture can be found in the R-S Encoder data sheet [Ref 15] and R-S Decoder data sheet [Ref 16].

Convolutional Encoder

The Convolutional Encoder feature set is as follows:

- High-speed compact convolution encoder with puncturing option
- Parameterizable constraint length from 3 to 9
- Parameterizable convolution codes
- Parameterizable puncture codes
- Puncturing rates from 2/3 to 12/13 available
- Incorporates Xilinx Smart-IP™ technology for
- Utmost parameterization and optimum implementation

This core is straightforward logic consisting of registers and XOR gates. Even though the core is capable of puncturing to support multiple puncturing rates, it is advised that the puncturing is done external to the core. Further details on the convolutional encoder architecture can be found in the Convolutional Encoder data sheet [Ref 17].

Interleaver/De-Interleaver

The interleaver/de-interleaver is used to minimize the effects of long burst errors. The feature set is as follows:

- Forney Convolutional and Rectangular Block type architectures available
- Easy-to-use interface signals
- Fully synchronous design using a single clock
- Symbol size from 1 to 256 bits
- Internal or external symbol RAM
- Incorporates Xilinx Smart-IP technology for maximum performance
- Parameterizable number of branches
- Parameterizable branch lengths
- Supports uniform and non-uniform branch length increments
- Multiple configurations with on-the-fly swapping
- Parameterizable, variable or selectable numbers of rows and columns
- Parameterizable or variable block size (can change numbers of rows/columns or block size at start of each new block)
- Row and column permutations
- Multiple permutations for selectable rows or columns

The interleaver/de-interleaver is based on the Forney algorithm. Further details on the architecture and functionality of the core can be found in the Interleaver/De-interleaver data sheet [Ref 18].

Viterbi Decoder

This core implements a Viterbi Decoder for decoding convolutionally encoded data. For details of the encoding process, see the "Convolutional Encoder." The decoder core consists of two basic architectures: a fully parallel implementation, which gives fast data throughput at the expense of silicon area, and a serial implementation, which occupies a small area but requires a fixed number of clock cycles per decoded result. The feature set is as follows:

- Fully synchronous design using a single clock
- Parameterizable constraint length from 3 to 9
- Parameterizable convolution codes
- Parameterizable traceback length
- Decoder rates from 1/2 to 1/7
- Parallel architecture with Area or Speed optimizations
- Very low latency option
- Minimal block RAM requirements; two block RAMs for a constraint length 7 decoder
- Serial architecture for small area
- Soft decision with parameterizable soft width
- Multi-channel decoding
- Dual rate decoder
- Trellis mode
- Erasure for external puncturing

- BER monitor
- Normalization
- Synchronization
- Best state option
- Trellis Initialization options for packet handling
- Direct traceback options for packet handling

As stated earlier, the Viterbi decoder can either be configured to trade off area versus performance. If there are a number of channels to be processed, then the decoder can be used in a multi-channel configuration without the expense of implementing multiple decoders. Further details on the architecture and functionality of the core can be found in the Viterbi decoder data sheet [Ref 19].

DVB-S2 FEC Encoder

The DVB-S2 FEC Encoder core provides a complete Forward Error Correction (FEC) encoding solution for DVB-S.2. Figure 21 illustrates a block diagram of the main blocks: the Outer (BCH), Inner (LDPC) encoding, and bit-interleaving stages.
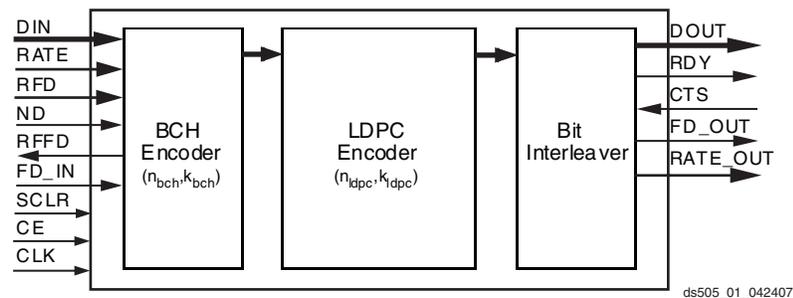

Figure 21: **Xilinx DVB-S2 FEC IP Core**

The core is also buffered on both the input and the output. The encoder supports all rates and both normal and short frames. Each encoding stage adds a number of bits dictated by the coding rate (where each *k* and *n* in Figure 4 refers to the number of input and output bits at each stage, respectively). The final number of coded output bits (*nldpc*) is 64,800 for a normal frame and 16,200 for a short frame. The bit interleaver supports the interleaving required by all modulation types, which may be QPSK, 8PSK, 16APSK, or 32APSK. All parameters can be changed on a frame-by-frame basis. To increase the throughput of the core, the input and output data word length can be widened to 4 bits. Internal processing of the data is carried out in parallel for the 4-bit input option. The feature set is as follows:

- Compatible with ETSI EN 302 307 V1.1.1
- Normal and short frames
- All code rates
- Input and output buffer, BCH outer coding
- LDPC encoder and bit-interleaver
- Fully optimized for speed and area
- Fully synchronous design using a single clock.

More details on the core are available in the DVB-S2 FEC data sheet [Ref 20].

Implementation of FEC IP in Xilinx FPGAs

The Xilinx CORE Generator™ software delivers a library of parameterizable and fixed netlist LogiCORE IP cores with corresponding data sheets, all designed and supported by Xilinx. The CORE Generator can be accessed as a standalone tool or from the Xilinx ISE design environment.

Generating a core, be it any of the Xilinx FEC cores (that is, Reed-Solomon Encoder/Decoder, Convolutional Encoder, Interleaver/De-interleaver, Viterbi Decoder, or DVB-S2 FEC) is straightforward. Use the new keyword search function to find a core, then specify the desired parameters and simply click a button to generate it. The output is an optimized core for the targeted FPGA device family that includes the following files:

- A tailored Xilinx implementation netlist
- VHDL or Verilog instantiation code
- VHDL or Verilog wrapper for simulation support
- A symbol for schematic capture tools

Up-front FPGA resource estimates are provided to help the user determine the best FPGA for the project. The Xilinx CORE Generator is supported on all ISE platforms.

The CORE Generator IP library can also be used to implement other sections of the various standards that have been reviewed in this paper. Two of the major components are the OFDM multiplexing for terrestrial TV and the baseband shaping filters that are required in the modulation and demodulation sections of all standards.

OFDM transmission is based on an inverse FFT, and a forward FFT in the receiver. This can be implemented using Fast Fourier Transform IP cores available from Xilinx. The IP has the ability to change from forward to inverse transform, switch between different transform sizes to support the various numbers of carriers used in different DTV transmission systems, and to support and apply different scaling.

The FIR Compiler IP allows the ability to assess the frequency response of the coefficients before designing the baseband shaping filter and allow the reconfiguration of the filter with new coefficients if required.

Not all FEC and channel coding system blocks require an IP core. For instance, the energy dispersal blocks, implemented using a simple pseudo random binary sequence (PRBS) scrambler, can easily be implemented in FPGA logic. In fact, Xilinx FPGAs offer enhanced functions, such as the SRL16E, which is a highly optimized 16-bit shift register implemented in a single LUT, and these are ideal for constructing PRBS scramblers while using negligible logic resources.

Using System Generator for DSP or AccelDSP™ Synthesis Tool

System Generator for DSP is a highly productive design environment for the development and prototyping of DSP systems using FPGAs. See Figure 22 and Figure 23. System Generator enables the use of The Mathworks Simulink®/MATLAB modeling environments for FPGA design by providing a Xilinx specific blockset for use within the Simulink modeling environment. DSP algorithm developers who do not know RTL design techniques can quickly capture their designs and accelerate their simulations using pushbutton hardware co-simulation flows.

AccelDSP™ Synthesis Tool is a high-level MATLAB language based tool for designing DSP blocks for Xilinx FPGAs. The tool automates floating-to-fixed-point conversion, generates synthesizable VHDL or Verilog, and creates a test bench for verification. The

user can also generate a fixed-point C++ model or System Generator block from a MATLAB algorithm

Both of these tools provide an alternative design path for implementing broadcast FEC and modulation designs in Xilinx FPGAs. By offering such alternatives, the user can design in the environment that is most comfortable and can build systems without necessarily having to learn completely new FPGA design methodologies and hardware design languages, but still have access to the high performance architecture.
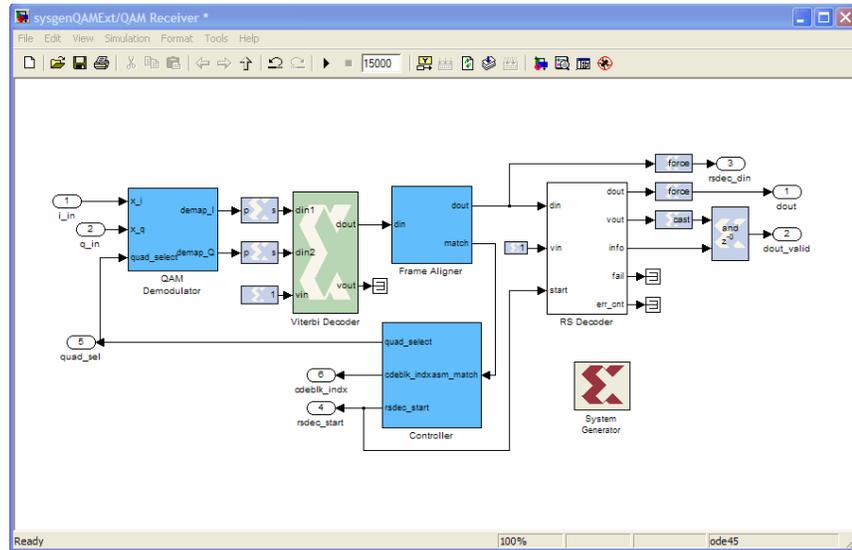

Figure 22: **Design Environment for System Generator**

Figure 23: **Design Environment for AccelDSP**

Summary and Conclusion

This paper has provided an overall view of the digital television broadcast standards and has outlined how Xilinx helps to meet the FEC requirements, in particular, and DSP requirement, in general, by offering a fully flexible and reprogrammable way of implementing standard blocks with changeable parameters.

Xilinx offers fully parameterizable FEC cores for Reed-Solomon, Convolutional Encoding, Viterbi Decoding, Interleaving and De-Interleaving. In certain cases, some of the hard work has already been done—a drop down menu in the Xilinx core generating software allows selection of the DVB or the ATSC option, and all the parameters are automatically filled to the DVB or ATSC specification for certain FEC blocks. Alternatively, the intuitive GUI allows the users to specify their own values to support other broadcast standards.

Xilinx has a complete range of parameterizable FEC IP available to suit user applications. These cores give users the flexibility of being able to quickly modify systems should new standards appear or evolve, and they also provide high-performance, scaleable solutions allowing the incorporation of more channels in fewer devices than current ASSPs allow, greatly lowering the overall cost-per-channel, as outlined in the BDTI's report [Ref 21]. Furthermore, the FEC may be replaced by improved algorithms in next generation specifications. As the FEC implementation need not take up all the resources in an FPGA, the user could also have space for integrating extra system functions, such as other DVB blocks, DSP filters, network interfacing, MPEG co-processing, and, of course, the user's own designs.

A programmable solution means that such modifications can be done quickly and even remotely, so no costly board re-spins, hardware upgrades, or field technician's time are required. Xilinx FPGA-based FEC solutions gives the user faster time-to-market and a greater competitive edge.

For further details, or technical support on the Xilinx FEC portfolio, or any of the digital TV broadcast offerings, please contact the local Xilinx sales person or send an e-mail to espteam@xilinx.com.

Appendix – FEC Implementation Details in Xilinx FPGAs

Table 2:   **Virtex-4 FPGA Forward Error Correction Resources**

Function	Device	Slices	Block RAMs	% Slices	% Block RAMs	Speed (MHz)
Reed-Solomon Encoder	XC4VLX60-10	122	0	1	0	295
Reed-Solomon Decoder	XC4VLX60-10	761	2	2	1	150
Interleaver	XC4VLX60-10	130	1	1	1	169
Viterbi Decoder	XC4VLX60-10	2084	2	7	1	168

Table 3:   **Virtex-5 FPGA Forward Error Correction Resources**

Function	Device	Slices	Block RAMs	% Slices	% Block RAMs	Speed (MHz)
Reed-Solomon Encoder	XC5VLX30-1	66	0	1	0	415
Reed-Solomon Decoder	XC5VLX30-1	376	2	7	3	201
Interleaver/De-interleaver	XC5VLX30-1	70	1	1	3	207
Viterbi Decoder	XC5VLX30-1	728	2	15	3	205

Table 4:   **Spartan-3 FPGA Forward Error Correction Resources**

Function	Device	Slices	Block RAMs	% Slices	% Block RAMs	Speed (MHz)
Reed-Solomon Encoder	XC3S4000-4	124	0	1	0	170
Reed-Solomon Decoder	XC3S4000-4	784	2	2	2	100
Interleaver/De-interleaver	XC3S4000-4	130	1	1	1	115
Viterbi Decoder	XC3S4000-4	2184	2	7	2	88

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17. Xilinx Convolutional Encoder Data Sheet:

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18. Xilinx Interleaver/De-Interleaver Data Sheet:

    www.xilinx.com/support/documentation/ip_documentation/sid_ds250.pdf

19. Xilinx Viterbi Decoder v6.0 Data Sheet:

    www.xilinx.com/support/documentation/ip_documentation/viterbi_ds247.pdf

20. Xilinx DVB-S2 FEC Data Sheet:

    www.xilinx.com/support/documentation/ip_documentation/dvb_s2_fec_encoder.pdf

21. BDTI Focus Report: FPGAs for DSP, Second Edition

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/05/07	1.0	Initial Xilinx release.
04/21/08	1.0.1	Updated links to reference 17, 18, 19, and 20.

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