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Designing Nx100G Applications with Heterogeneous 3D FPGAs

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To address the insatiable demand for bandwidth, the communications industry is accelerating development of Nx100G line cards for networking systems. For equipment manufacturers to scale infrastructure economically and effectively, they must leverage the latest optical interconnect technologies such as CFP2, and in the future CFP4, to increase bandwidth while lowering power and cost.

By working with network developers, Xilinx anticipated this need and developed transceiver-rich, high-performance, programmable devices comprised of heterogeneous silicon die. The technology supports 28 gigabits per second (Gb/s) transceivers for CFP2 optics and delivers optimal signal integrity due to its heterogeneous architecture. With high logic capacity and specific IP for communications applications, the latest Xilinx devices provide extensive levels of system integration to usher in the migration to next-generation optics.

The Demand for Bandwidth

Largely driven by streaming video, HD video, cloud computing, and mobile networking, the consumer market's relentless demand for network bandwidth compels the communications industry to double system capacity every three years. Service providers supporting the Internet's backbone must lead the migration to 100G and 400G and stay at the forefront of the latest technologies and standards.

Service providers not only demand more bandwidth but aim to reduce capital and operating expenses. For equipment manufacturers, this means rolling out solutions with leaps in performance, area efficiency, and cost effectiveness over previous generation products.

The Move to Next-Generation Optics for Nx100G

Most of today's network infrastructure is connected via optical fiber, hence the bandwidth and cost of optical modules are major development considerations. The type of modules that can be used depends on the architecture of the application's line cards. Three well known optical module standards include SFP+, CFP, and CFP2—each with varying throughput, cost per bit, power efficiency, and form factor:

- Small form factor pluggable (SFP+) optical modules support 10G optical links and are currently shipping in high volume.
- 100G form factor pluggable (CFP) modules, also in production, support 100G optical links. Though they consume more power per bit than SFP+, integration to a single 100G fiber greatly reduces complexity and serviceability costs.
- The CFP2 optical module offers the same 100G bandwidth as a CFP, but in half the space at a reduced cost, and consumes half to two-thirds less power than a CFP module.

Because of the 2X bandwidth-per-watt efficiency gained from CFP2 modules over CFP, the industry is eager to move to these optics. Without this technology, the cost of migrating to 100G is prohibitive for many service providers. The need for CFP2 is demonstrated in Figure 1, showing a comparison of optical interfaces as they appear on the faceplate connector of a fixed-width line card. Because service providers postpone upgrading their chassis until economically feasible, network OEMs must strive to provide more capabilities within the same unit area and power envelope. Scaling bandwidth within existing infrastructure is driven by throughput per watt per unit area of optical ports.

When using SFP+ optical modules to connect 10G optical links, the top faceplate connector shown in Figure 1 can accommodate 48 fiber links. The arrangement in this example provides 480 Gb/s of throughput.

Comparatively, four CFP ports can be designed in the same footprint of 48 SFP+ modules. With each CFP accommodating a single 100G fiber link, this provides a total of 400 Gb/s of bandwidth. Though there is a slight increase in power, the integration reduces complexity and serviceability.

A CFP2 module, by contrast, provides the same 100G bandwidth of a CFP in half the width while consuming half the power per 100G port. In this example, within the same area, a module could accommodate eight CFP2 ports for an aggregate 800 Gb/s bandwidth within the same power envelope. This is 33% higher bandwidth and power efficiency compared to SFP+ and double the efficiency provided by CFP modules.

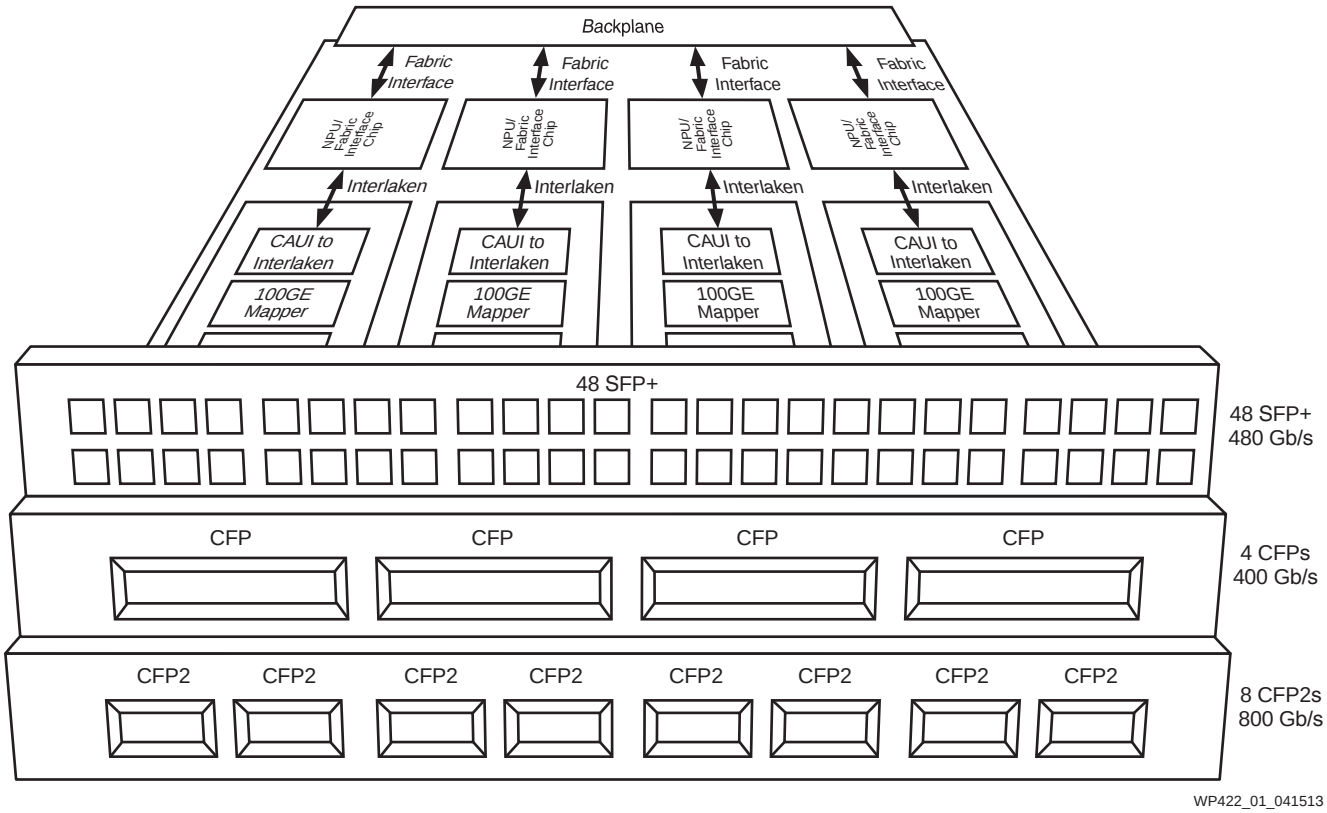

Figure 1: **Throughput for Line Cards and Face Plate Connectors of Fixed Width**

The Challenge of Redesigning the Line Card for Nx100G

Migrating to CFP2 has its benefits, but the need for higher density face plates poses challenges on the line card itself. Effective integration is needed on the silicon side to support the incoming bandwidth so as not to nullify the power and cost efficiencies promised by a CFP2 transition.

A typical line card with a 100G transponder is shown in Figure 2, with an optical interface at one end and a backplane interface at the other. Typically, there is a forward error correction (FEC) block to minimize packet retransmission and framing and mapping functions to handle data transport. Interfaces such as CAUI and Interlaken are also used.

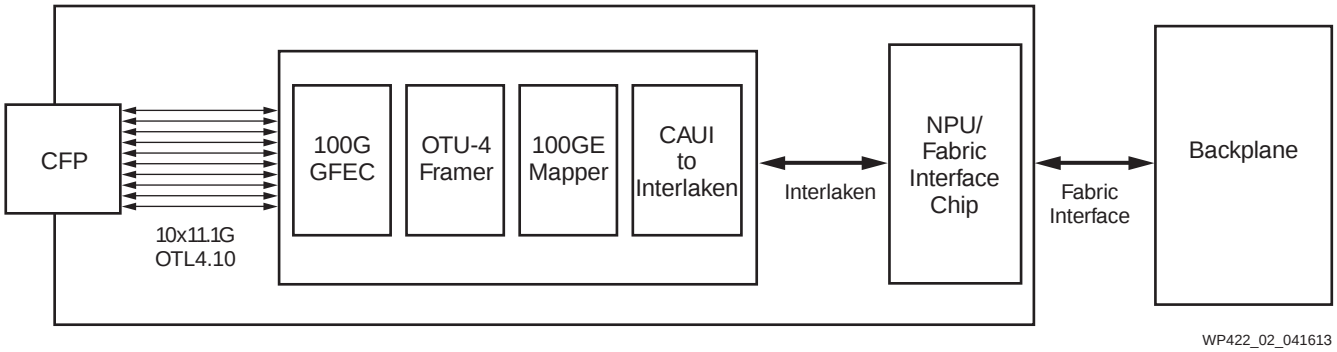

Figure 2: **Line Card with 100G Transponder**

To redesign the line card for 2X bandwidth, the interface to CPF2 must first be considered, given that it can support 4x25G channels (as well as 10x10G pass-through mode) versus CFP modules that can only support 10x10G channels.

Using simple bit-multiplexing, a functional block known as a "gearbox" can convert a 100G interface comprised of 4x25G channels into 10x10G channels, allowing these modules to interface with existing silicon infrastructure. Consequently, the original devices that operate via 10x10G do not necessarily need to be replaced to support CFP2. The gearbox maps data between the ten and four serial lane interfaces, in both ingress and egress directions. It converts data streams of either four lanes of CAUI4 (4x 25.78G) or OTL4.4 (4x 27.95G) to CAUI (10x 10.3125G) or OTL4.10 (10x 11.18G).

Although the gearbox addresses optics connectivity, it still does not address the 2X bandwidth. If the CFP is replaced by two CFP2 modules, the system either has to support additional components of similar type within the same area or support completely new silicon to support 2x100G throughput. Migrating to new silicon architectures can be prohibitive in terms of cost and schedule, and a new implementation using similar components has its own challenges. A re-design of the line card to support 2x100G using similar components and gearbox ASSPs is shown in Figure 3. The increased number of components requires more area on the PCB. Even if such a layout is feasible, the increase in cost and power consumption can nullify the advantages of a CFP2 migration. Fortunately, next generation FPGAs provide an alternative.

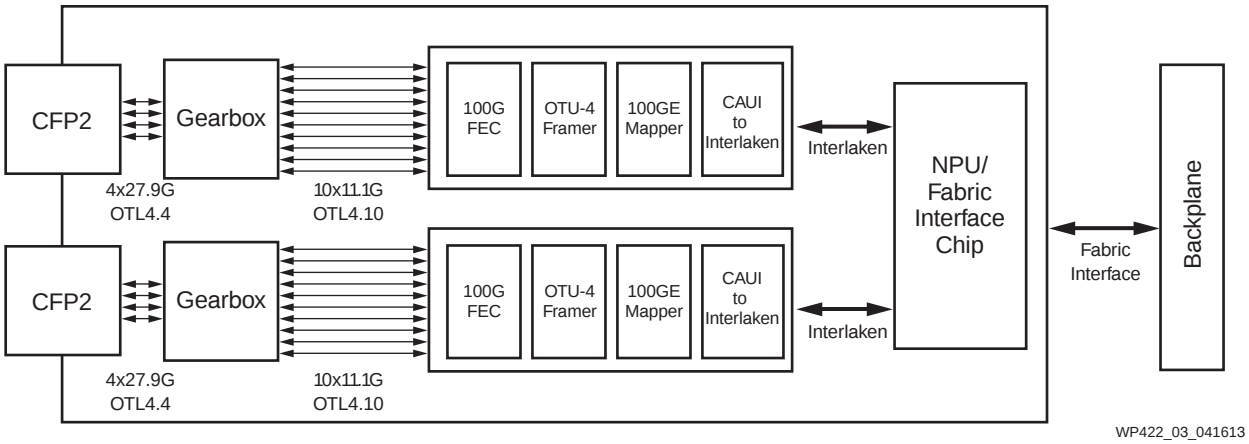

Figure 3: **Five Devices Required to Redesign Line Card to Support CFP2 and 2x100G**

28G Enabled FPGAs as a Solution

FPGAs play a critical role in networking equipment because of their flexibility and ability to rapidly implement the latest networking standards, even as these standards evolve. FPGAs have also evolved to meet next-generation networking requirements by delivering greater capacity, performance, and features, along with more robust transceivers supporting higher line rates.

To interface to CFP2 modules, FPGAs provide 25G–28G serial interfaces with support for advanced protocols and interface specifications. These include 100GE, OTU4, 400GE, CAUI, CAUI4, OTL4.4, SFI-S and other standards.

High line rate support is only half the challenge for successful 28G design. Signal integrity is another consideration at this transmission rate. The CEI-28G specification

guiding the electrical specifications for 28G imposes very tight transmit jitter budgets (0.28 UI) on system designers and requires robust equalization techniques in the receiver to build 28G chip-to-optics interfaces.

An FPGA Tailored for Wired Communications Applications

Xilinx Virtex®-7HT FPGAs were designed to match these unique requirements, addressing the bandwidth needs, signal integrity challenges, and integration demands. As a single chip solution enabling Nx100G applications, the Virtex-7 HT FPGA ushers in the transition to CFP2 optical modules.

Based on Stacked Silicon Interconnect Technology

The Virtex-7 family is based on 3D Stacked Silicon Interconnect (SSI) technology, which combines enhanced FPGA die slices, known as Super Logic Regions (SLRs), and a passive silicon interposer to create a three dimensional die stack. This interposer implements tens of thousands of die-to-die connections to provide ultra-high inter-die bandwidth with lower power consumption and one fifth the latency of standard I/Os. The Virtex-7 HT device shown in Figure 4 ties together three SLRs fabricated on 28 nm. Next to these SLRs are separate 28G transceiver (GTZ) die. Because of its 3D nature, SSI technology has allowed the Virtex-7 family to outpace Moore's law in performance, capacity, and power efficiency. For more information, refer to WP380, *Xilinx Stacked Silicon Interconnect Technology Delivers Breakthrough FPGA Capacity, Bandwidth, and Power Efficiency.*

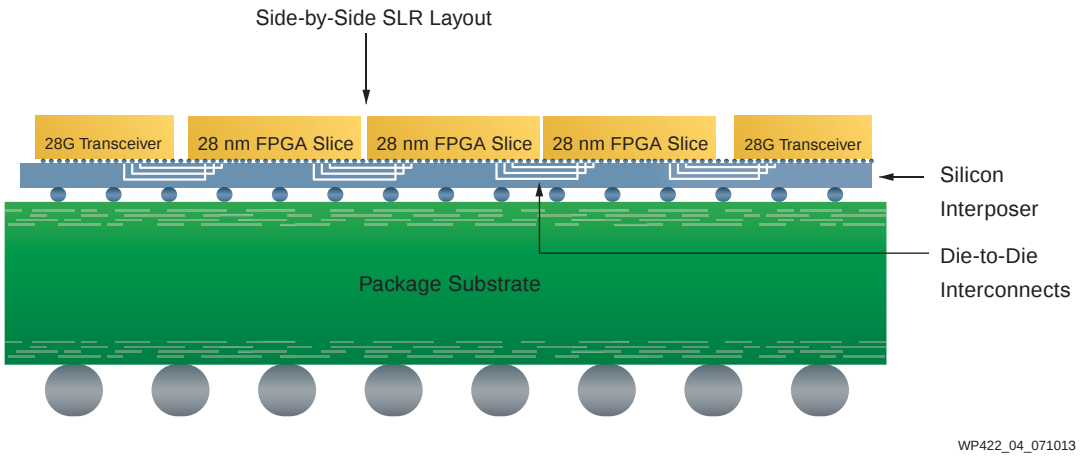

Figure 4: **Xilinx Stacked Silicon Interconnect Technology (Side View)**

Heterogeneous Silicon for Low Jitter and Noise Isolation

The Virtex-7 HT FPGA uses SSI technology with traditional FPGA SLR slices and 28 Gb/s transceiver slices to create the world's first heterogeneous device.

The transceiver's superior jitter performance is enabled by a narrowly tuned phase-locked loop (PLL) based on an LC tank design. Unique clocking, clock distribution, and PLL design minimizes jitter across multiple transceivers. For example, rather than sharing a PLL via a high-speed multiplexor, each TX or RX channel has a dedicated LC tank PLL. Additional design features minimize lane-to-lane skew to support tough optical standards like the Scalable SerDes Framer Interface (SFI-S). In addition to superior PLL design, the transceiver's jitter

performance is further improved through noise isolation inherent in the device's architecture.

Xilinx employs a unique approach to isolate the digital logic from the analog transceiver circuit on the same interposer, as shown in Figure 5—in essence, placing heterogeneous die side-by-side to operate as one integrated device. If this were a monolithic device, the approach of competing solutions, the digital logic region would create a noisy environment that degrades transceiver performance. The electrical isolation of the digital and analog circuits in a heterogeneous device allows for low noise and jitter. The noise isolation architecture provides a considerable reduction in noise coupling compared to traditional approaches. This simplifies the job of PCB and layout engineers, accelerates 28G design closure, and reduces board cost.

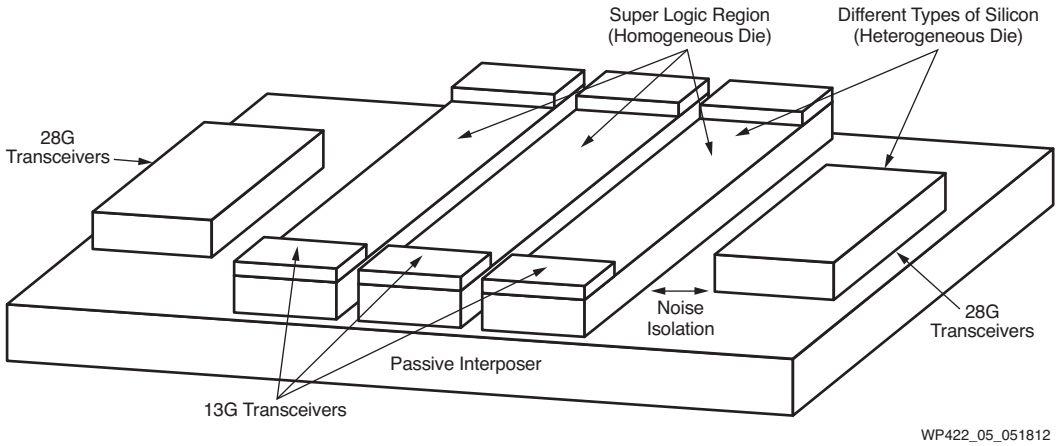

Figure 5: **Heterogeneous 3D FPGA Enables Low Jitter 28G Transceiver Design**

To compensate for channel loss and maintain signal integrity, Xilinx 28G transceivers employ a programmable main transmit driver, programmable transmit pre-emphasis, and an auto adapting continuous time linear equalizer (CTLE) in the receiver.

The eye diagram in Figure 6 demonstrates the low jitter and high signal quality of the 28G FPGA transceiver on the Virtex-7 XC7VH580T device. The 28G GTZ transceiver presents an almost ideal eye, with clean edges and no over-equalization.

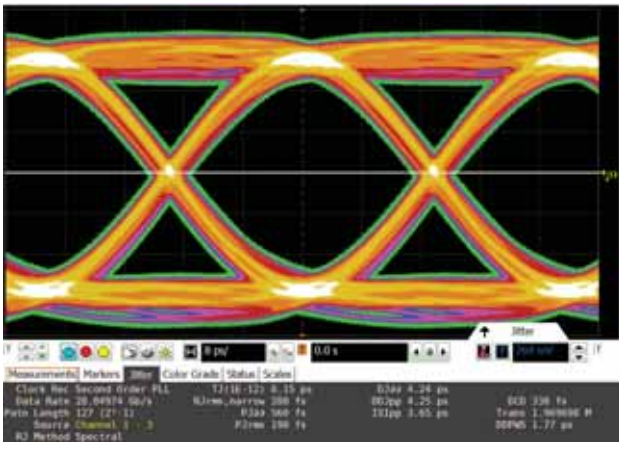

Figure 6: **28 Gb/s Eye Diagram of GTZ Transceiver on the Virtex-7 H580T FPGA**

An FPGA with up to 2.78 Terabits per Second of Bandwidth

The heterogeneous architecture also enables an unprecedented number of transceivers on Virtex-7 HT devices. The devices offer two types of serial transceivers:

- GTH transceivers operate up to 13.1 Gb/s and support optical, chip-to-chip, and backplane connectivity.
- GTZ transceivers deliver up to 28.05 Gb/s for 100G optical networking.

The Virtex-7 XC7VH870T device offers up to sixteen 28G transceivers—4X the competition—making it uniquely matched to interface to up to four CFP2 modules for 4x100G applications or 400 Gigabit Ethernet.(1) With an additional seventy-two 13.1 Gb/s GTH transceivers on the same device, system designers have multiple options for chip-to-chip connectivity, including Interlaken, Ethernet, and OTN. With up to 88 transceivers overall, the Virtex-7 HT device is the highest bandwidth FPGA available, providing 2.78 terabits per second (Tb/s) of throughput. Competing alternatives, whether FPGA or ASSPs, have up to only four 25–28G transceivers, allowing for only 100 Gb/s per device.

Gearbox IP to Enable System Integration

As important as CFP2 connectivity is, the intellectual property (IP) cores needed for the line cards are equally critical. Xilinx provides gearbox IP that handles 4x25G to 10x10G conversion. It also supports a 10x10G-to-10x10G pass-through mode for designs that need to support both CFP and CFP2.

While a single Virtex-7 HT FPGA can provide up to 4x100G throughput via its gearbox IP connecting to up to four CFP2 ports, competing FPGA or ASSP solutions can provide only 100G throughput on a single device. As already shown in Figure 3, if an ASSP approach were taken to upgrade the line card, separate gearbox chips would be needed, thereby increasing cost, power consumption, and board complexity.

Programmable Silicon Integration for a Single-Chip Solution

The other benefit of using the Virtex-7 HT FPGA is flexibility when integrating IP. Designers can take integration to the next level by combining gearbox, Ethernet MAC, OTN transponder, OTN muxponder, differentiating IP, and standard or proprietary chip-to-chip or backplane interfaces (e.g., XAUI, Interlaken) within the FPGA.

A Comparison of Two Transponders

A 2x100G line card is shown in Figure 7, where a Virtex-7 HT device is used to integrate multi-chip functionality. The simplicity of this architecture is in stark contrast to the alternative in Figure 3. A designer can implement four of these Virtex-7 HT devices, producing an 8x100G system that can interface with eight CFP2 ports. An equivalent scaling of the alternative implementation in Figure 3 would require at least *16 devices* —consuming excessive area, increasing PCB cost and power, and likely lengthening the project schedule.

1. Special considerations are required regarding OTL 4.4 dynamic skew. Contact Xilinx for more information.

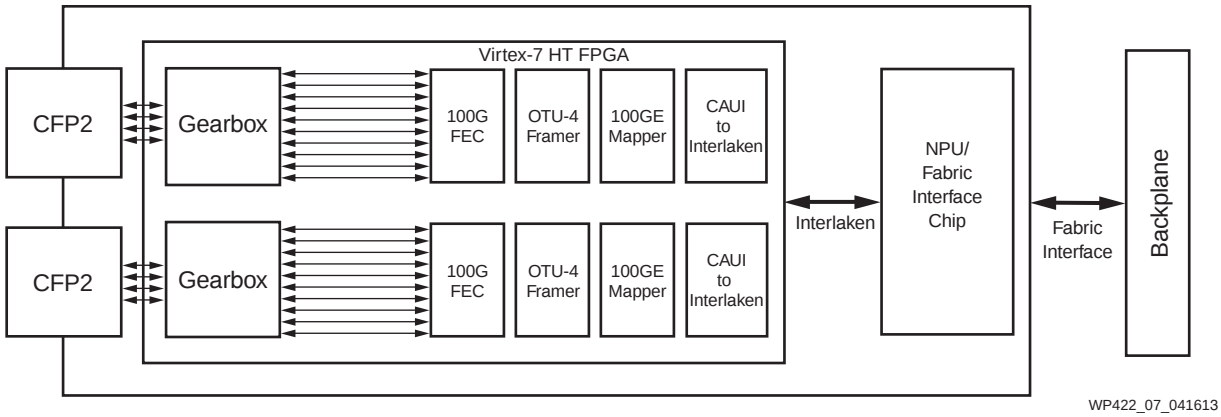

Figure 7: **Line Card with 2x100G Transponder Using a Virtex-7 HT FPGA**

Logic resources and types of applications for Virtex-7 HT devices are shown in Table 1. Due to its capacity and number of 28G transceivers, the Virtex-7 XC7VH870T is currently the only silicon on the market capable of implementing a 400 Gigabit Ethernet solution. Hence, while there is currently no 400GE standard, the device is 400GE-ready.

Table 1: **Virtex-7 HT Family and Key Types of Applications**

	XC7VH580T	XC7VH870T
Logic Cells	580,480	876,160
GTH Transceivers (13G)	48	72
GTZ Transceivers (28G)	8	16
Types of Applications	2x100G	4x100G or 1x400G

Enabling CFP2 Connectivity and Beyond

The market need for higher-bandwidth networking line cards and next-generation optics is real. Xilinx is at the forefront of this movement with a heterogeneous architecture that provides the bandwidth and capacity for adopters of 100G, based on CFP2 optics. Without an FPGA solution of this caliber, the migration would not only be sub-optimal, but costly. By leveraging FPGAs, designers get a level of integration that is two-fold: optical connectivity at the system level and IP integration at the silicon level. By targeting Virtex-7 HT devices, designers achieve the greatest possible port density, protect themselves against evolving standards, and prepare themselves for optics even beyond CFP2.

Additional Information

To learn more about the Virtex-7 HT devices, go to the 28 Gb/s Serial Transceiver Technology webpage on xilinx.com:

http://www.xilinx.com/technology/roadmap/28g-serial-transceiver-technology.htm

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
05/29/12	1.0	Initial Xilinx release.
07/22/13	1.1	Updated the white paper title and abstract. Updated: The Demand for Bandwidth, The Move to Next-Generation Optics for Nx100G, including Figure 1, The Challenge of Redesigning the Line Card for Nx100G, including Figure 2 and Figure 3, 28G Enabled FPGAs as a Solution, Based on Stacked Silicon Interconnect Technology, including Figure 4, Heterogeneous Silicon for Low Jitter and Noise Isolation, including Figure 6, An FPGA with up to 2.78 Terabits per Second of Bandwidth (previously titled: Highest Bandwidth FPGA with up to 88 Transceivers), Gearbox IP to Enable System Integration (previously titled Gearbox IP to Enable CFP2), Programmable Silicon Integration for a Single-Chip Solution, A Comparison of Two Transponders, including Figure 7 and Table 1, and Enabling CFP2 Connectivity and Beyond. Removed Power/Cost of ASSP Implementation vs. FPGA-Based 8x100G Line Card table (previously Table 1).

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